Technical information

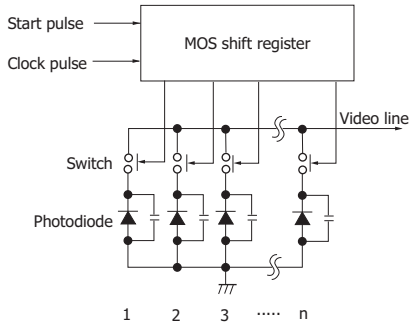
Current output type
CMOS linear image sensors with variable integration time function
S10121 to S10124 series

1 Features

In previous current output type NMOS linear image sensors, once a readout starts, the internal shift register scans the readout switches from the first pixel to the last pixel to read out all the pixels, and therefore the integration times of all pixels are the same.
With current output type CMOS linear image sensors with variable integration time function, a readout control circuit is used to control the shift register output making it possible to read out only specific pixels and set an appropriate integration time for each pixel.
When a CMOS linear image sensor is used in a spectrometer and the like, light dispersed according to wavelength enters each pixel. The level of light entering each pixel is different. The variable integration time function can be used to set a long integration time for pixels with low incident light levels and short integration time for those with high incident light levels to enable measurements with high S/N over a wide spectral range.

[Figure 1] Block diagram

(a) NMOS linear image sensor (S3901 to S3904 series)



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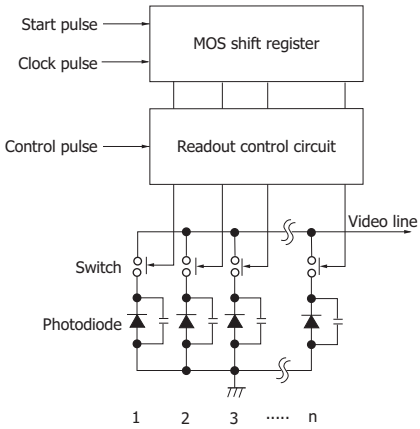
(b) CMOS linear image sensor (S10121 to S10124 series)



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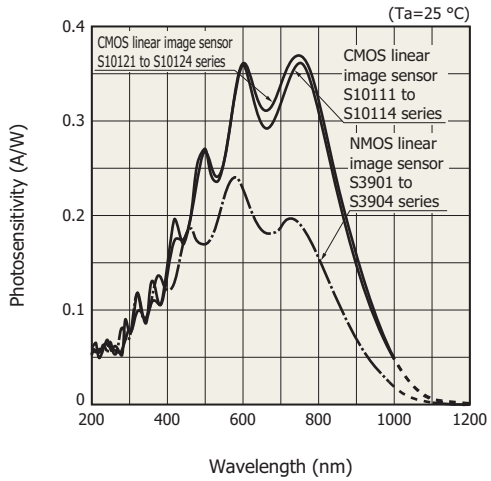
[Table 1] Comparison of NMOS linear image sensors and CMOS linear image sensors

Product name	NMOS linear image sensor (S3901 to S3904 series)				CMOS linear image sensor (S10121 to S10124 series)			
Features	●High UV sensitivity ●Excellent output linearity ●Low power consumption				●High UV sensitivity ●Smoothly varying spectral response characteristics in UV region ●Excellent output linearity ●Low power consumption ●Variable integration time for each pixel ●Large saturation charge			
Application	Spectrophotometry				Spectrophotometry			
Type no.	S3901	S3902	S3903	S3904	S10121	S10122	S10123	S10124
Number of pixels	128, 256, 512		256, 512, 1024		128, 256, 512		256, 512, 1024	
Pixel pitch [µm]	50		25		50		25	
Pixel height [mm]	2.5	0.5	0.5	2.5	2.5	0.5	0.5	2.5
Saturation charge [pC]	50	10	5	25	140	28	14	70
Peak sensitivity wavelength [nm]	600				750			
Power consumption across Vdd and Vss [mW]*1	-	-	-	-	0.75 1.75 4.25	1.5 3.5 8.25	3.25 7.25 18.25	1.75 3.75 8.25

*1: f(CLK)=250 kHz (S10121/S10124 series), 500 kHz (S10122/S10123 series)

[Figure 2] Spectral response (typical example)

(a) 200 to 1200 nm



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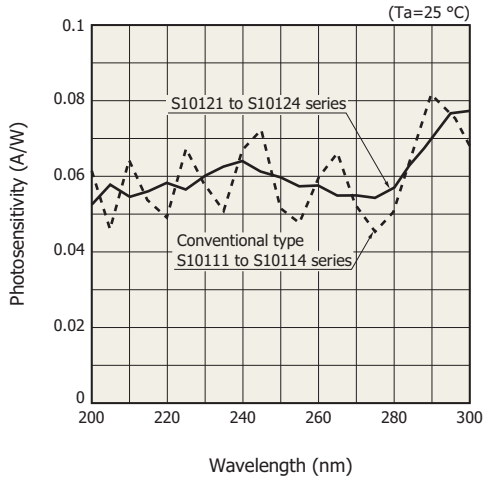
(b) Ultraviolet region



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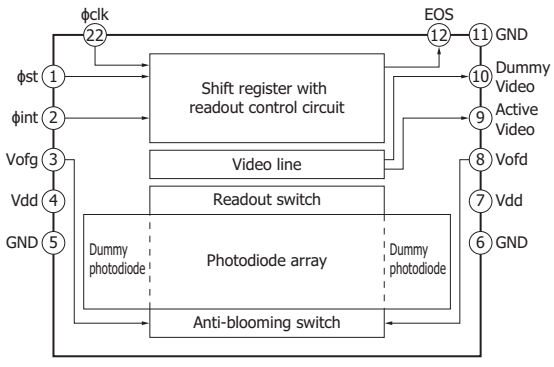
[Figure 3] Device structure

(a) Block diagram



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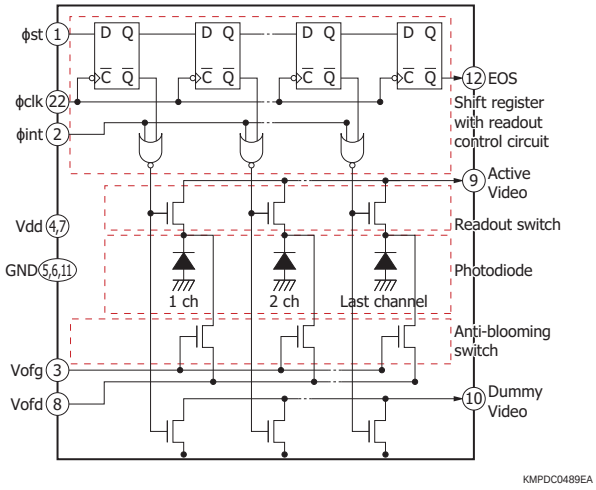
(b) Equivalent circuit



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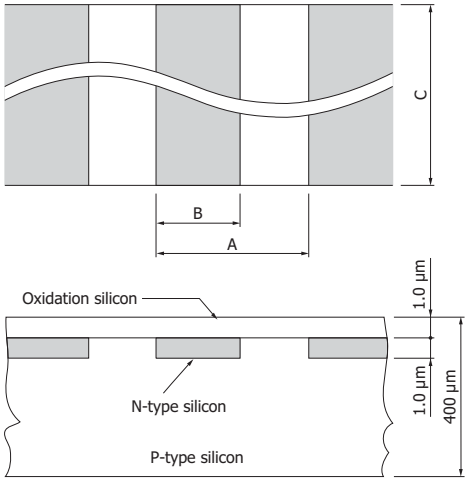
2 Description of each section

(1) Photodiode (photosensitive area)

The photosensitive area is made up of PN junction photodiodes, which are composed an N-type diffusion layer formed on a P-type silicon substrate. It serves as a photoelectric converter that converts light signals into electrical signals and also temporarily stores the obtained signal charges. Vss is connected to the anode of each photodiode. The photodiode is designed to provide high UV sensitivity but low dark current. Figure 4 shows a structure diagram of the photosensitive area. “A” indicates the photodiode pixel pitch; “B” indicates the width of the photodiode diffusion layer; “C” indicates the photodiode height.

[Figure 4] Structure of photosensitive area



	A	B	C
S10121 series	50 µm	45 µm	2.5 mm
S10122 series			0.5 mm
S10123 series	25 µm	20 µm	0.5 mm
S10124 series			2.5 mm

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(2) Readout switches

The readout switch is made up of an address switch array, which is composed of N-channel MOS transistors whose source is the photodiode cathode, drain is the video line, and gate is the address pulse input. Each photodiode is connected to the active video line via an address switch. The address pulse from the shift register turns on the address switch and causes the output signal to appear in the video line. The readout switch ON resistance is approximately 500 Ω.

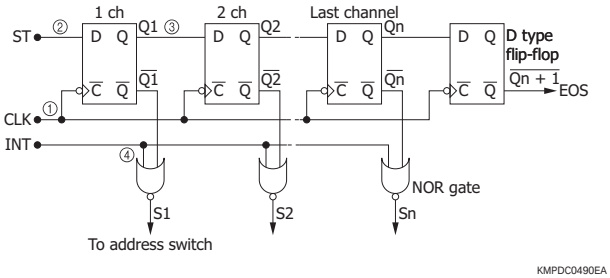
(3) Anti-blooming switches

The anti-blooming switch is made up of switches, which are composed of N-channel MOS transistors whose source is the photodiode cathode, gate is the overflow gate, and drain is the overflow drain.
When a light level higher than the saturation exposure enters a photodiode, the photodiode cannot store a signal charge in excess of the saturation charge. The excess signal charge overflows and diffuses into the adjacent photodiodes and the video lines, resulting in deterioration of signal purity, so-called "blooming."
An anti-blooming switch is provided in the S10121 to S10124 series for each photodiode separately from the normal signal output line connected to the video line, in order to allow the excess charge to bleed off.

(4) Shift register with readout control function

The shift register with readout control function is composed of a D type flip-flop for every channel plus one extra D type flip-flop and NOR gates [Figure 5].
The CLK signal is input to pin C of each D type flip-flop of every channel that makes up the shift register (①), and the ST signal connected to pin D of the ch 1 D type flip-flop (②). The D type flip-flop retains the input to pin D as output of pin Q on the falling edge of the CLK signal. Pin Q of ch 1 is connected to pin D type of ch 2 (③), and this pattern is repeated to the last channel. Applying ST and CLK signals externally causes the D type flip-flop circuit to operate, and the signal is output from each channel in order from ch 1.
Furthermore, to allow readout control, the inverted signal from pin Q and the INT signal are input to the two input terminals of each NOR gate (④). The on and off of the address switch of each channel can be controlled using the INT signal.
When the readout of all pixels is complete, an EOS (end-of-scan) pulse is output at the next timing after the last pixel.

[Figure 5] Circuit of shift register with readout control function



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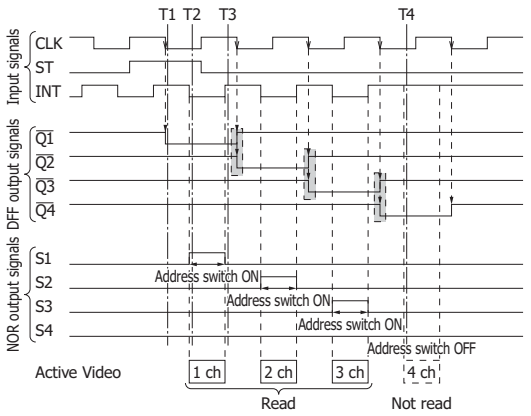
The INT signal and the output from the D type flip-flops enter the NOR gates. When consecutive pixels are read out, a high-level period must be provided in the INT signal to prevent the shift register output of adjacent pixels from turning on simultaneously in the gray area of Figure 6, in order to ensure only a single pixel is turned on. The INT signal must be set to high level for at least 30 ns before and after the CLK falling signal. However, this is not necessary during the period between an EOS and the next rising edge of the ST signal.

3 Timing chart

Figure 6 shows a timing chart of the shift register section. The CLK signal is changed from high level to low level once during the high-level period of ST. This starts the operation of the D flip-flops making up the shift register.

[Figure 6] Shift register operation



$\overline{QX}$: Pin $\overline{Q}$ output of X ch
SX: NOR gate output of X ch

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· T1

CLK changes to low level, and $\overline{Q1}$ changes to low level. Since the INT signal is at high level, S1 remains at low level.

· T2

When the INT signal changes to low level while $\overline{Q1}$ is at low level, S1 changes to high level, and the readout switch of the ch 1 shift register turns on.

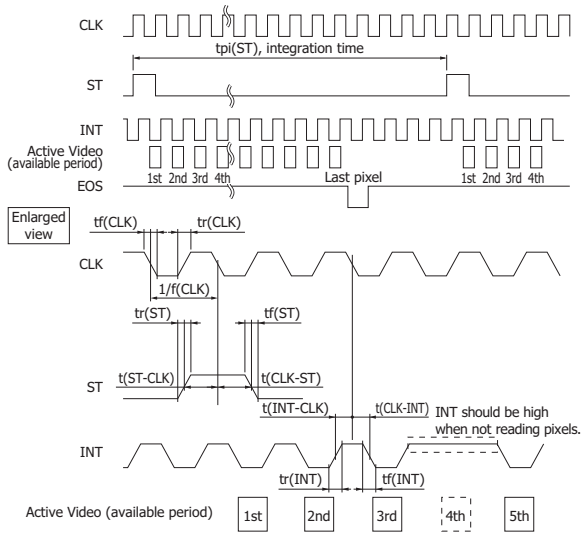
· T3

$\overline{Q1}$ is at low level. When the INT signal changes to high level, S1 changes to low level, and the readout switch of the ch 1 shift register turns off.

· T4

$\overline{Q4}$ is at low level. When the INT signal is at high level, S4 remains at low level, and the readout switch of the ch 4 shift register remains off.

[Figure 7] Timing chart



Parameter		Symbol	Min.	Typ.	Max.	Unit
Start pulse (ST) cycle	S1012*-128	tpi(ST)	130/f(CLK)	-	-	s
	S1012*-256		258/f(CLK)	-	-	
	S1012*-512		514/f(CLK)	-	-	
	S1012*-1024		1026/f(CLK)	-	-	
INT pulse rise and fall times		tr(INT), tf(INT)	0	20	30	ns
INT pulse - clock pulse timing		t(INT-CLK)	30	-	1 / [2 × f(CLK)]	ns
Clock pulse - INT pulse timing		t(CLK-INT)	30	-	1 / [2 × f(CLK)]	ns
Start pulse rise and fall times		tf(ST), tr(ST)	0	20	30	ns
Clock pulse duty ratio		-	40	50	60	%
Clock pulse rise and fall times		tf(CLK), tr(CLK)	0	20	30	ns
Clock pulse - start pulse timing		t(CLK-ST)	20	-	-	ns
Start pulse - clock pulse timing		T(ST-CLK)	20	-	-	ns

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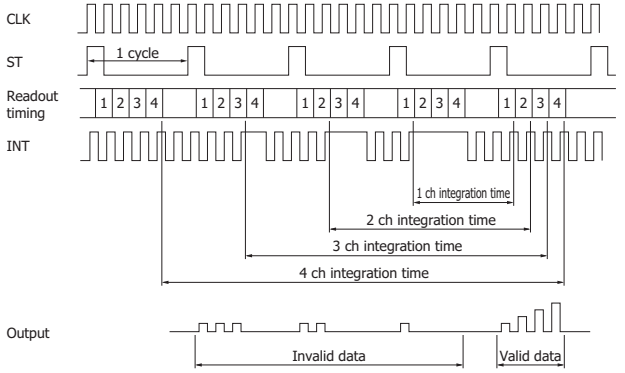
4 Variable integration time function

Controlling CLK of pin INT makes it possible to change the integration time of each pixel to "an integer multiple of the readout cycle." If CLK of pin INT is set to high level at the readout timing of a specific pixel, the signal for that pixel is not output [Figure 8]. If the signal from the specified pixel is not output, integration continues for that pixel. For example, if the integration time of a readout cycle is 100 ms and this function is used to output a signal every three cycles for a specific pixel, the integration time for that pixel is 300 ms. Increasing the integration time of a specific pixel makes it possible to efficiently detect low-level wavelength component signals of dispersed light.

The timing chart of the variable integration time function is shown in Figure 8. Here, an example is provided for a case where the integration times of the second, third, and fourth pixels are set to twice, three times, and four times the integration time (one cycle of the start pulse) of the first pixel. The integration time can be varied for each pixel by applying INT pulse as shown in figure 8.

[Figure 8] Timing chart (variable integration time function)



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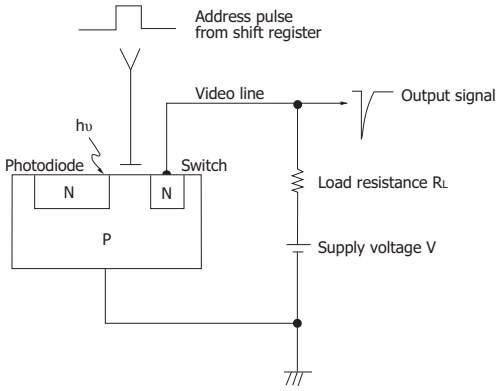
5 Operating principle

Figure 9 shows the setup of a photodiode and readout switch for a single pixel. Figure 10 shows the equivalent circuit of the setup. The details of the readout operation are explained below.

The photodiode is a PN junction photodiode consisting of an N-type diffusion region formed on a P-type silicon substrate. The readout switch is made up of N-channel MOS transistors whose source is the photodiode cathode, drain is the the video line side, and gate is the address pulse input from the shift register. The photodiode anode (silicon substrate) is connected to GND, and the video line is biased at the positive potential Vb.

When an address pulse from the shift register enters the gate of the readout switch, the switch turns on. As a result, the photodiode cathode is set to the same potential as the video line, and the photodiode is initialized to a reverse-bias state. At this point, the photodiode junction capacitance Cj is supplied with a charge, Qj = Cj × Vb, from the power supply. When the switch turns off and integration starts, the stored charge is discharged by the charge generated by the incident light, and the cathode potential approaches GND potential. The amount of discharge increases in proportion to the incident light level, but the maximum amount is limited by the amount of charge initially stored. This corresponds to the saturation charge. When an address pulse is received again and the readout switch turns on, a charge equal to the that discharged during the integration time is supplied from the power supply through the load resistance RL, so that the photodiode is initialized again. At this point, a potential difference due to the charge current appears across the load resistance RL, and is detected as an output voltage. This output has a differential waveform with a negative polarity with respect to the video line bias voltage Vb. This signal readout method is called current-to-voltage conversion, and its simplified operating diagram is shown in Figure 11.

[Figure 9] Structure of readout section



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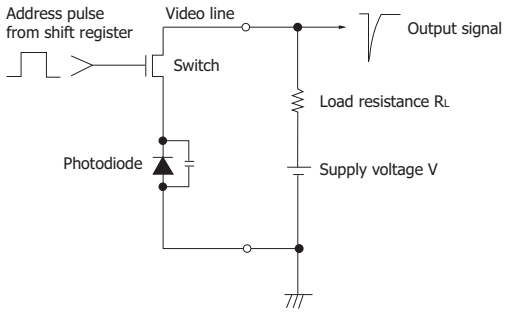
[Figure 10] Equivalent circuit of current-to-voltage conversion method



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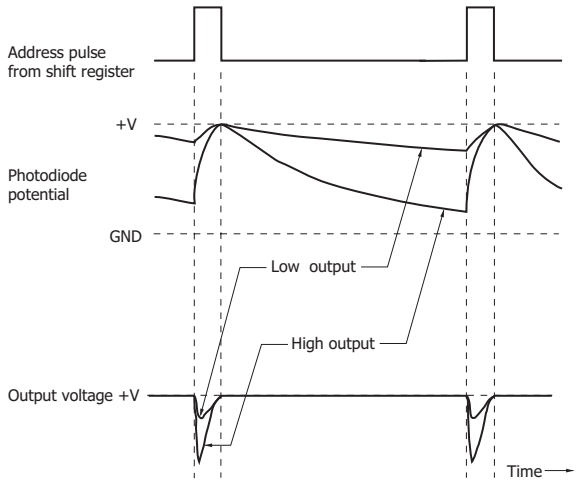
[Figure 11] Operation of current-to-voltage conversion method



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In actual operation, the stored charge gradually discharges due to the re-combination current and the surface leakage current in the depletion layer in addition to the photocurrent described above. These currents that are unrelated to the illumination of light are referred to as dark current and its output is called dark output.

6 External current integrating driver circuit example

As shown in Figure 12, a driver circuit consisting of a timing signal generator, video signal processor, voltage regulator, and so on must be prepared. The timing signal generator generates pulses required by the sensor, signal processor, and so on. The video signal processor performs current integration, amplification, and DC restoration on the video signals received from the sensor. The voltage regulator generates Vofd (=Vb) and Vofg.

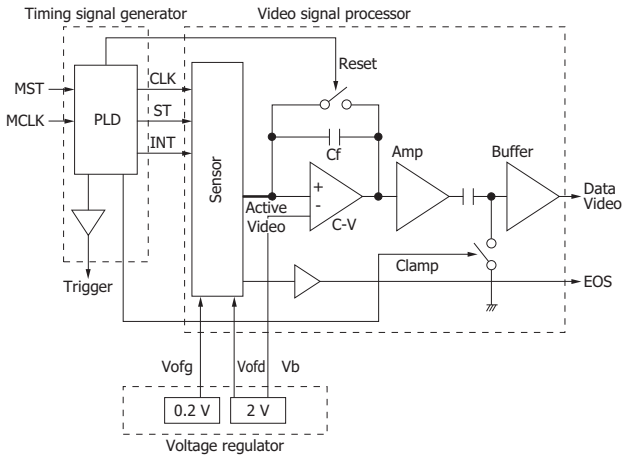
Digital supply voltage, analog supply voltage, master clock pulse, and master start pulse are applied to the driver circuit from external sources. On the other hand, the driver circuit outputs data video signal, trigger pulse, and EOS pulse.

The timing signal generator consists of a PLD (programmable logic device) and transmits (1) clock pulse and start pulse to operate the sensor shift register, (2) reset signals to the current integrating circuit to process output signals, and (3) clamp signal to the DC restoration circuit. The generator also provides a trigger output signal for external sample-and-hold and transmits it via a buffer. These signals are synchronized with an external master clock pulse and are initialized by an external master start pulse.

The video signal processor comprises four sections: first-stage amplifier, second-stage amplifier, clamp circuit, and last-stage amplifier. The first stage amplifier integrates the video output current from the sensor. Video bias voltage Vb (=Vofd) is applied to the non-inverting input terminal of the first stage amplifier. A reset switch is connected in parallel with the integration capacitor, so that the capacitance is reset by a reset signal input to the switch each time a pixel is read out. The first stage amplifier also cancels the switching noise that is synchronized to the clock pulse. The first stage amplifier output, which is a positive boxcar waveform with respect to the 2 V video bias, is given by equation (1). Denoting the output voltage (unit: V) as V and the output charge (unit: pC) as Q,

$$V = Q/Cf \cdots\cdots(1)$$

[Figure 12] External driver circuit example



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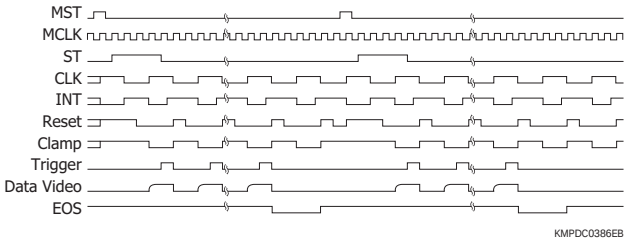
The second-stage amplifier performs non-inverting amplification. Then, a clamp circuit composed of a capacitor and switch performs CDS (correlated double sampling). The clamp switch is turned on for a given period (clamp period) immediately after the integration capacitance is reset in order to fix the clamp circuit output potential to ground. This eliminates the reset noise that occurs in the integration capacitance reset switch. The last-stage non-inverting amplifier transmits

data video signals.
The voltage regulator generates two voltages: Vofg and Vofd. Vofg is applied to the MOS transistor gate, and therefore hardly any current flows to pin OFG. The current that flows through pin OFD depends on the over-saturated state. Up to several tens of mA may flow. To use in a over-saturated state, the drive capability must be increased to allow current to flow through pin Vofd.

[Figure 13] Timing chart example of external driver circuit

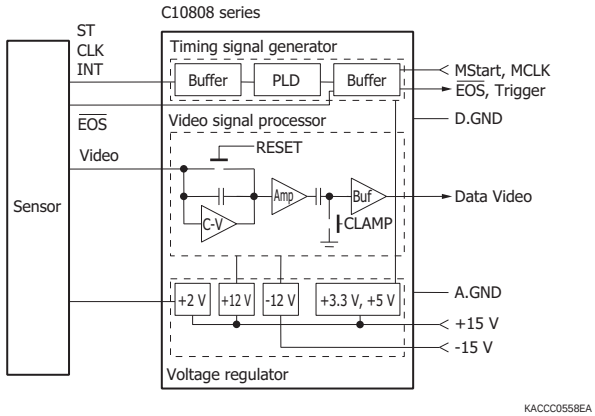


Precautions when configuring the driver circuit

- Separate the analog circuit ground and the digital circuit ground.
- Connect the video output terminal to the amplifier input terminal in the shortest possible distance.
- When wiring, avoid crossing of analog and digital signals or running them in parallel as much as possible.
- Use a series power supply having only small voltage fluctuations.

Hamamatsu provides the C10808 series as a driver circuit for the CMOS linear image sensor S10121 to S10124 series. For details on the C10808 series, refer to the datasheet.

[Figure 14] Block diagram (C10808 series)



7 Q&A

What is the difference between the CMOS linear image sensor S10121 to S10124 series and the NMOS linear image sensor S3901 to S3904 series?

See the comparison table of Table 1. The S10121 to S10124 series feature large saturation charge and variable integration time function. In addition, a smooth spectral response is achieved in the ultraviolet region [Figure 2 (b)].

How should the dummy video terminal be used?

The dummy video terminal outputs only the switching noise component. The dummy video terminal is used in the current-to-voltage conversion method, but this method is not recommended because obtaining highly accurate readout is difficult. Note that the dummy video terminal is not used when the current integrating readout circuit is used.

What is the voltage Vb that is listed in the condition column of electrical characteristics?

Vb is a video bias voltage for using the current integrating readout method; there is no terminal on the image sensor for Vb. See Figure 12, which provides an connection example of the integrating circuit and Vb. Vb is a voltage for the non-inverting input terminal of the integration amplifier. It is a reset voltage for the photodiode.

Is it necessary to operate Vb and Vofd at the same voltage?

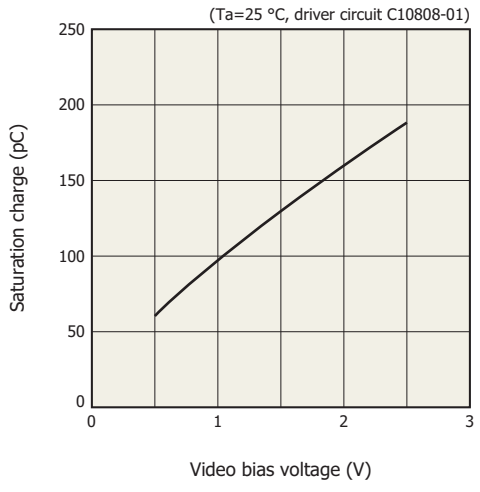
Normally, operate Vb and Vofd at the same voltage. Vofd is connected to the drain of the overflow-drain MOS transistor. An equivalent circuit is shown in Figure 3 (b). In the over-saturated state, current flows from Vofd to the photodiode. For example, if 100000 *lx*, an extremely intense light, is incident, several tens of milliamperes of current flows. Therefore, we recommend a circuit in which an op amp is connected as a buffer.

What is the optimum voltage for video bias voltage Vb?

A measurement example of a video bias voltage and saturation charge is shown in Figure 15. The video bias voltage ranges from 0.5 V to 2.5 V and is typically 2 V.

[Figure 15] Video bias voltage vs. saturation charge (typical example)

(a) S10121-512Q



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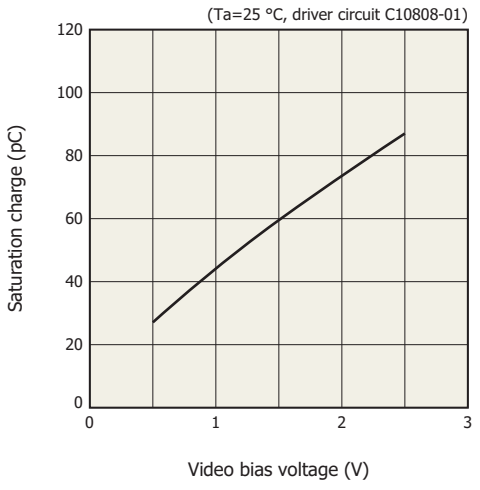
(b) S10124-1024Q



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◉ Is it necessary to set the overflow gate voltage Vofg to 0.2 V? Is there a problem with using 0 V? Also, is it okay to apply the voltage through a resistor divider?

The saturation charge is influenced by variance in Vofg. The larger the Vofg, the smaller the saturation charge. Since Vofg is connected to the anti-blooming MOS transistor gate in the sensor, it is at high input impedance and hardly any current flows. Therefore, there is no problem in applying Vofg through a resistor divider. Using Vofg at 0 V will cause problems such as increased time lag (unread signals) and deterioration in the sensitivity uniformity between pixels at near saturation output. To prevent these problems, use Vofg at 0.2 V.

◉ To what light levels does the overflow prevention function (anti-blooming function) work?

Under standard conditions, it has been confirmed that blooming does not occur up to 100 times the saturation exposure.

◉ Does the image sensor have sensitivity for light whose wavelength is 200 nm and less? If so, are there any points to consider when using the image sensor at such wavelengths?

The image sensor has some sensitivity for light whose wavelength is 200 nm and less, but it is outside the guaranteed range. Please use it at your own risk.

◉ How is the EOS pulse used?

The EOS pulse can be used to determine whether all the shift register stages are operating normally.

◉ How should the Cf value be set when using the current integrating readout circuit?

Set the value by considering the saturation output charge Qsat, the output voltage of the amplifier to be used, and so forth. For example, in the case of the S10121 series, if the saturation output charge Qsat is 140 pC and 5 V of amplitude relative to the video bias voltage can be provided for the output voltage of the op amp, Cf=Qsat/V=140 pC/5 V=28 pF.

◉ What are the points to consider when constructing a current integrating readout circuit?

Consider the following points if you are selecting ICs for the current integrating readout circuit.

① First-stage amplifier: For the first-stage amplifier, select an IC with low noise and low input bias current while considering the switching speed.

② Second- and third-stage amplifiers: Select amplifiers that can handle high load capacitance.

③ Reset switch and clamp switch: Use FET or analog switches. Select switches with minimal ON resistance and low reset noise and charge injection. Also, consider the signal voltage range.

◉ Are window materials other than the quartz window or windowless types supported?

Windowless types can be provided. Consult with your nearest Hamamatsu sales office. Please also consult us about window materials other than the quartz window.

◉ If all pixels are read out without using the variable integration time function, is it okay to leave the INT pulse at the low-level voltage?

The rising and falling edges of the internal pulse $\overline{Q}$ generated from the shift register overlap with the falling edges of the CLK signal [gray area in Figure 6]. If the INT pulse is kept at the low-level voltage at all times, there is a possibility that the readout switches of two pixels turn on simultaneously. Therefore, the INT pulse must be applied so that it is at high level for 30 ns before and after the CLK falling edges.

◉ Which section of the video signal should I refer to for the dark output reference?

Refer to the video output of each pixel during the dark states. This product does not have a dark output reference like the optical black of the CCD.

◉ What are the soldering conditions?

Use a soldering temperature of 260 °C or less, and perform the soldering within 5 seconds. This condition applies to a single pin. There is no problem in soldering multiple pins consecutively. We recommend that you grip the root of the lead you are soldering with tweezers or a similar tool to dissipate heat and prevent heat from conducting to the product package. As long as these conditions are met, there is no problem in using lead-free solder. This product does not support flow soldering.

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