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NEW

CMOS linear image sensor

S14739-20

High sensitivity, photosensitive area with vertically long pixels

The S14739-20 is a high sensitivity CMOS linear image sensor using a photosensitive area with vertically long pixels (14 × 200 μm). Other features include high sensitivity and high resistance in the UV region. The S14739-20 operates from a single 5 V supply making it suitable for use in low cost spectrometers. The surface mount type package allows reducing the mount area on a printed circuit board.

Features

- **Pixel size: 14 × 200 μm**
- **256 pixels**
- **Effective photosensitive area length: 3.584 mm**
- **High sensitivity: 1300 V/(lx·s)**
- **High sensitivity in UV to NIR region (spectral response range: 200 to 1000 nm)**
- **Simultaneous charge integration for all pixels**
- **Variable integration time function (electronic shutter function)**
- **5 V single power supply operation**
- **Built-in timing generator allows operation with only start and clock pulse inputs**
- **Video data rate: 10 MHz max.**
- **Surface mount type**

Applications

- **Spectrometers**
- **Position detection**
- **Image reading**
- **Encoders**

Structure

Parameter	Specification	Unit
Number of pixels	256	-
Pixel size	14 × 200	μm
Photosensitive area length	3.584	mm
Package	Ceramic	-
Window material	Quartz	-

Absolute maximum ratings

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd	Ta=25 °C	-0.3 to +6	V
Clock pulse voltage	V(CLK)	Ta=25 °C	-0.3 to +6	V
Start pulse voltage	V(ST)	Ta=25 °C	-0.3 to +6	V
Operating temperature	Topr	No dew condensation*1	-40 to +65	°C
Storage temperature	Tstg	No dew condensation*1	-40 to +65	°C
Reflow soldering condition	Tsol	JEDEC level 5	Peak temperature: 240 °C, 2 times (see P.8)	-

*1: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
Clock pulse voltage	High level	V(CLK)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	V
Start pulse voltage	High level	V(ST)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	V

Input terminal capacitance (Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse input terminal capacitance	C(CLK)	-	5	-	pF
Start pulse input terminal capacitance	C(ST)	-	5	-	pF

Electrical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(CLK)	200 k	5 M	10 M	Hz
Data rate	DR	-	f(CLK)	-	Hz
Output impedance	Zo	70	-	260	Ω
Current consumption*2 *3	Ic	5	15	35	mA

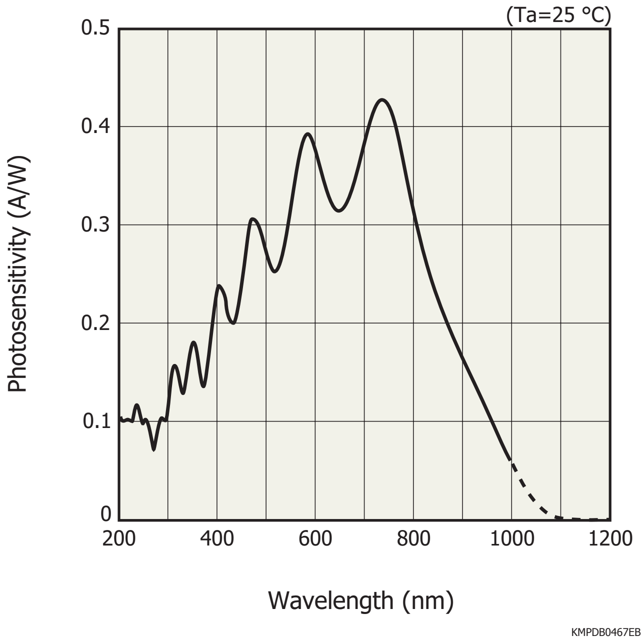
*2: f(CLK)=10 MHz
*3: Current consumption increases as the clock pulse frequency increases. The current consumption is 10 mA typ. at f(CLK)=200 kHz.

Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, V(CLK)=V(ST)=5 V, f(CLK)=10 MHz]

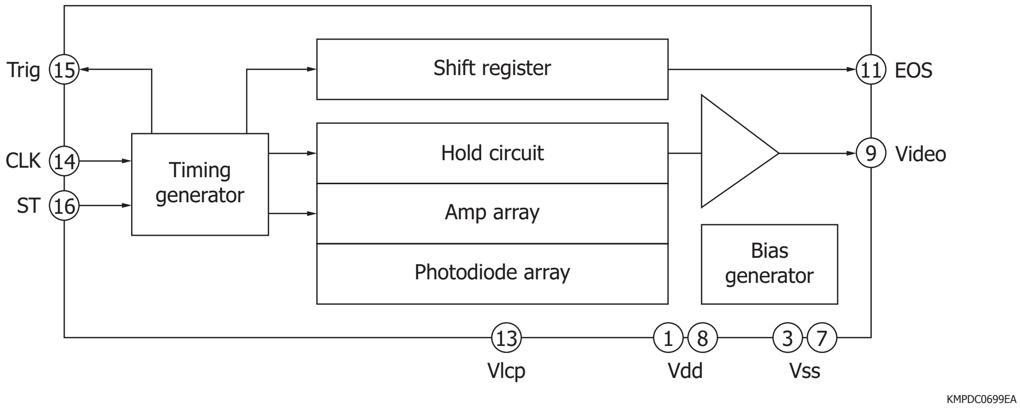
Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ		200 to 1000		nm
Peak sensitivity wavelength	λp	-	700	-	nm
Photosensitivity*4	Sw	-	1300	-	V/(lx·s)
Conversion efficiency*5	CE	-	25	-	μV/e⁻
Dark output voltage*6	VD	0	0.2	2.0	mV
Saturation output voltage*7	Vsat	1.5	2.0	2.5	V
Readout noise	Nread	0.1	0.4	1.2	mV rms
Dynamic range 1*8	Drange1	-	5000	-	times
Dynamic range 2*9	Drange2	-	10000	-	times
Output offset voltage	Voffset	0.3	0.6	0.9	V
Photoresponse nonuniformity*4 *10	PRNU	-	±2	±10	%
Image lag*11	Lag	-	-	0.1	%

*4: Measured with a tungsten lamp of 2856 K
*5: Output voltage generated per one electron
*6: Integration time=10 ms
*7: Difference from Voffset
*8: Drange1= Vsat/Nread
*9: Drange2= Vsat/VD
Integration time=10 ms
Dark output voltage is proportional to the integration time and so the shorter the integration time, the wider the dynamic range.
*10: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 250 pixels excluding 3 pixels each at both ends, and is defined as follows:
PRNU= $\Delta X/X \times 100$ (%)
X: average output of all pixels, ΔX: difference between X and maximum output or minimum output
*11: Signal components of the preceding line data that still remain even after the data is read out in a saturation output state.
Image lag increases when the output exceeds the saturation output voltage.

Spectral response (typical example)



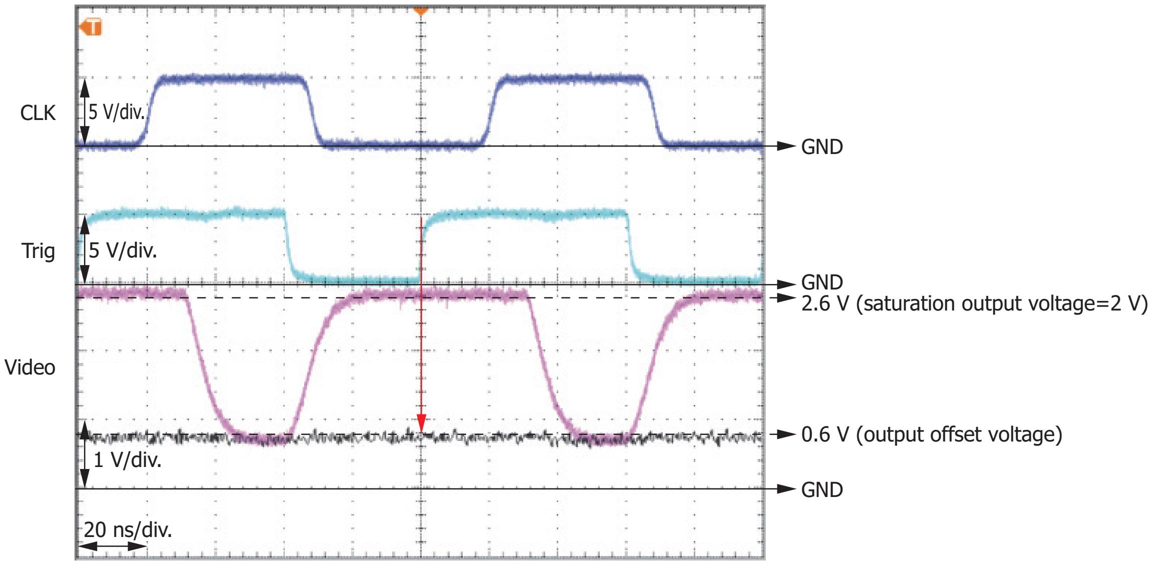
Block diagram



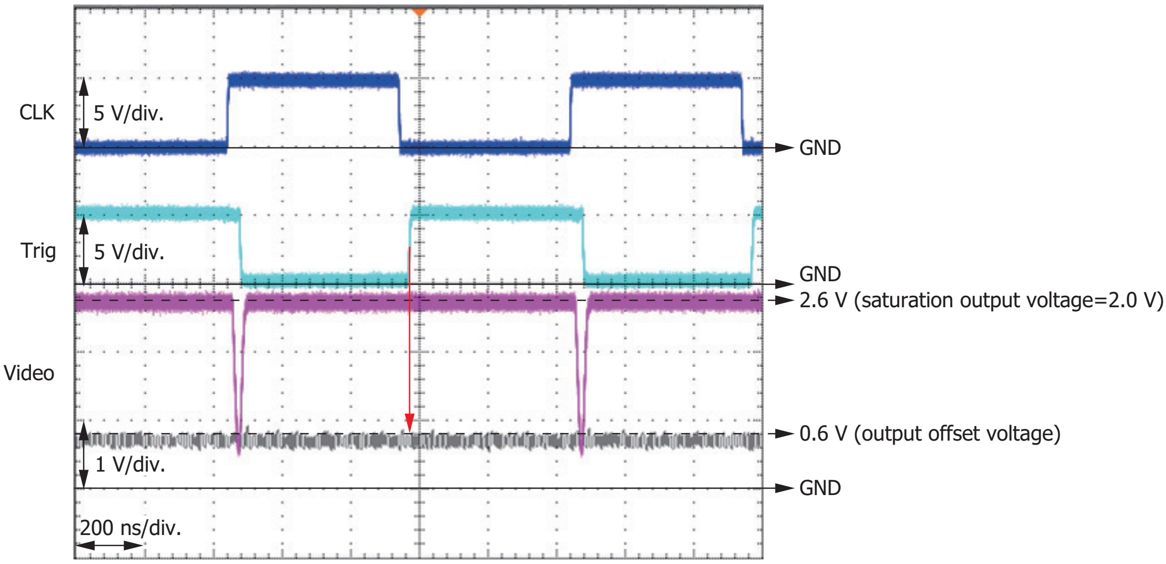
Output waveform of one pixel

The timing for acquiring the Video signal is synchronized with the rising edge of a trigger pulse (See red arrow below.).

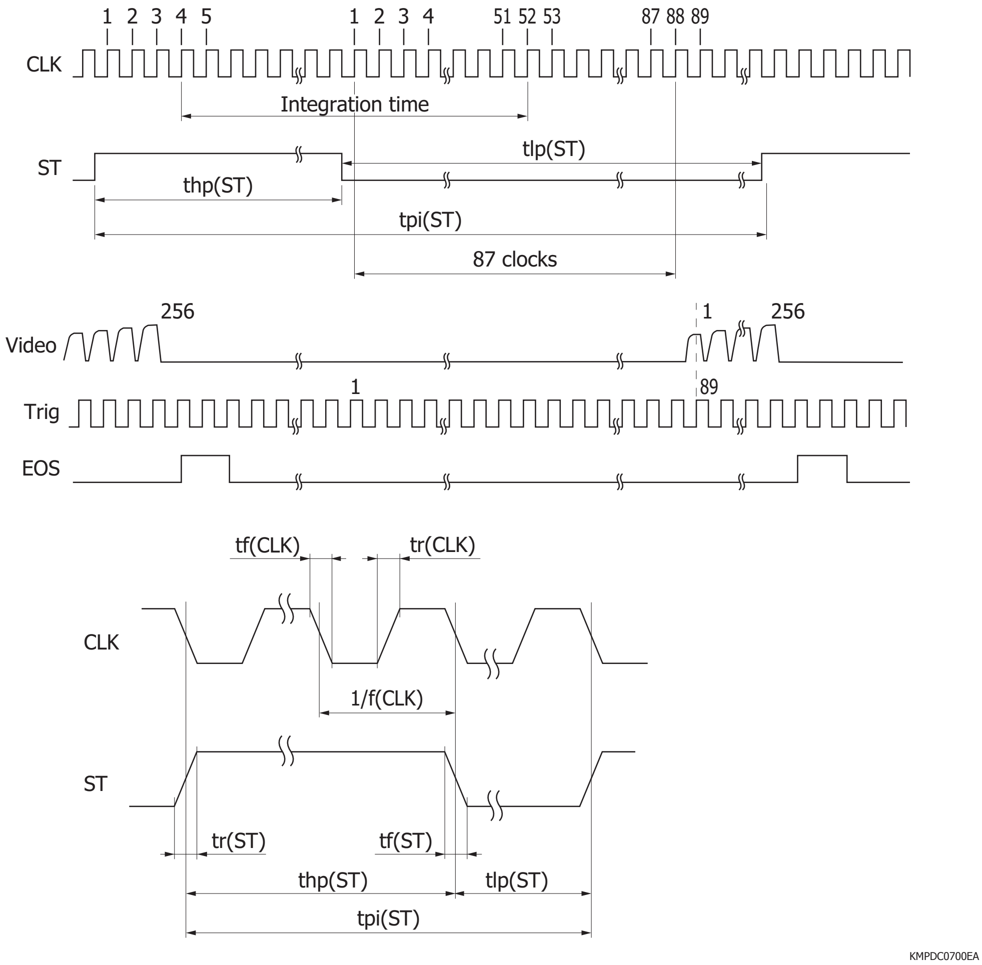
f(CLK)=DR=10 MHz



f(CLK)=DR=1 MHz



Timing chart

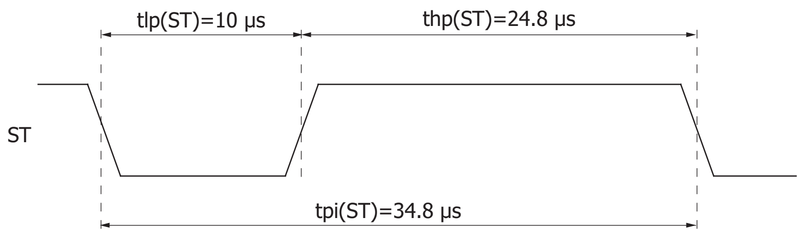


Parameter	Symbol	Min.	Typ.	Max.	Unit
Start pulse width interval*12	tpi(ST)	106/f(CLK)	-	-	s
Start pulse high period*12 *13	thp(ST)	6/f(CLK)	-	-	s
Start pulse low period	tlp(ST)	100/f(CLK)	-	-	s
Start pulse rise and fall times	tr(ST), tf(ST)	0	10	30	ns
Clock pulse duty	-	45	50	55	%
Clock pulse rise and fall times	tr(CLK), tf(CLK)	0	10	30	ns

*12: Dark output increases if the start pulse period or the start pulse high period is lengthened.
*13: The integration time equals the high period of ST plus 48 CLK cycles.
The shift register starts operation at the rising edge of CLK immediately after ST goes low.
The integration time can be changed by changing the ratio of the high and low periods of ST.
If the first Trig pulse after ST goes low is counted as the first pulse, the Video signal is acquired at the rising edge of the 89th Trig pulse.

Operation example

When the clock pulse frequency is maximized (video data rate is also maximized), the time of one scan is minimized, and the integration time is maximized (for outputting signals from all 2048 channels)
Clock pulse frequency = Video data rate = 10 MHz
Start pulse cycle = 348/f(CLK) = 348/10 MHz = 34.8 μs
High period of start pulse = Start pulse cycle - Start pulse's low period min.
= 348/f(CLK) - 100/f(CLK) = 348/10 MHz - 100/10 MHz = 24.8 μs
Integration time is equal to the high period of start pulse + 48 cycles of clock pulses, so it will be 24.8 + 4.8 = 29.6 μs.



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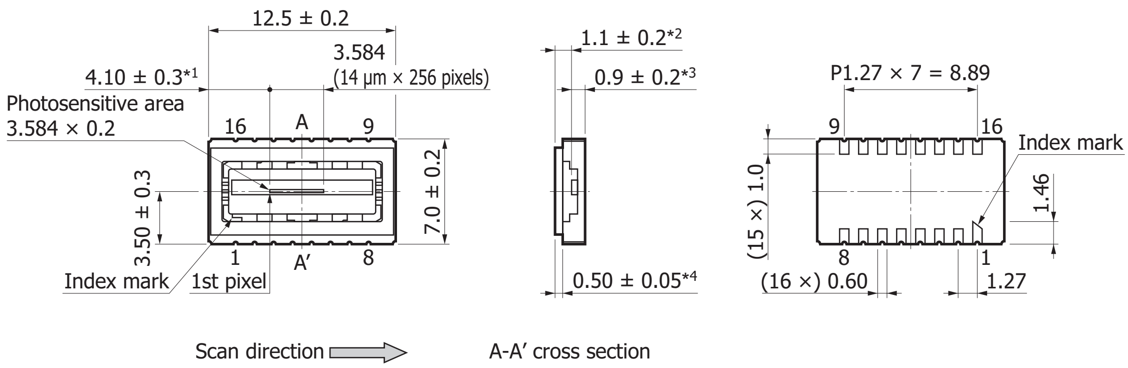
Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.2
*1: Distance from package edge to photosensitive area edge
*2: Distance from window upper surface to photosensitive surface
*3: Distance from package bottom to photosensitive surface
*4: Glass thickness

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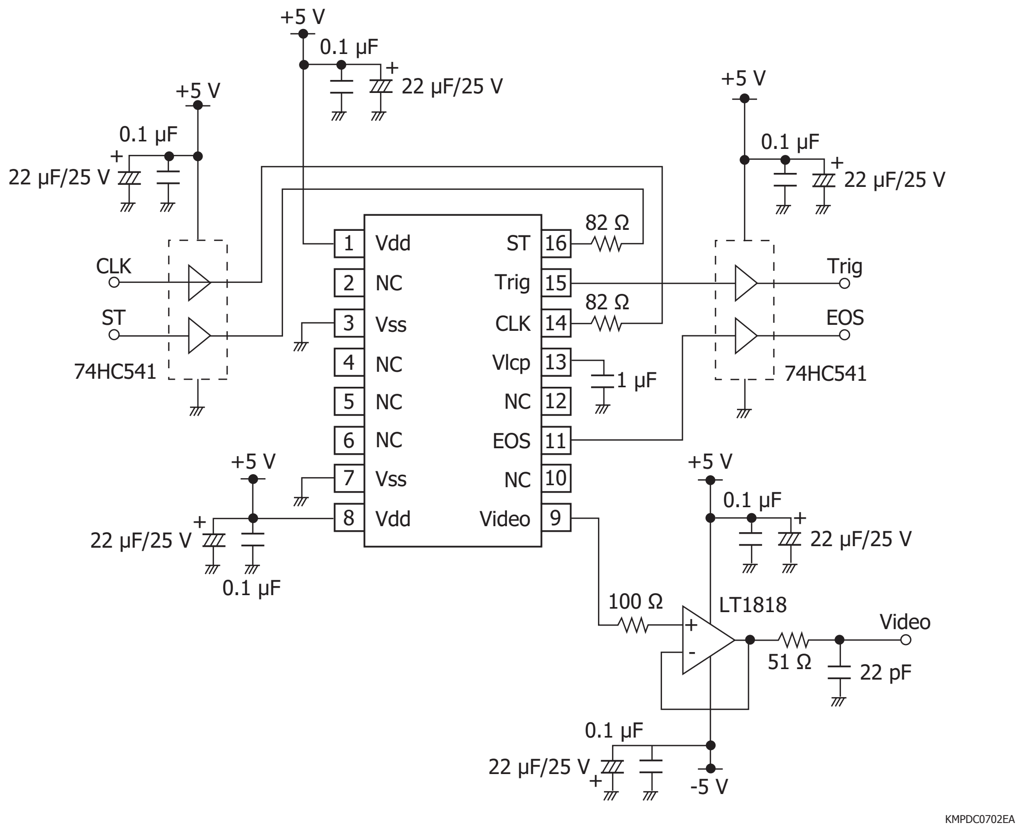
Pin connections

Pin no.	Symbol	I/O	Description	Pin no.	Symbol	I/O	Description
1	Vdd	I	Supply voltage	9	Video	O	Video signal*14
2	NC		No connection	10	NC		No connection
3	Vss		GND	11	EOS	O	End of scan
4	NC		No connection	12	NC		No connection
5	NC		No connection	13	Vlcp	O	Bias voltage for negative voltage circuit*15
6	NC		No connection	14	CLK	I	Clock pulse
7	Vss		GND	15	Trig	O	Trigger pulse for video signal acquisition
8	Vdd	I	Supply voltage	16	ST	I	Start pulse

*14: Connect a buffer amplifier for impedance conversion to the video output terminal so as to minimize the current flow. As the buffer amplifier, use a high input impedance operational amplifier with JFET or CMOS input.
*15: Approximately -1.5 V generated by the negative voltage circuit inside the chip is output to the terminal. To maintain the voltage, insert a capacitor around 1 µF between Vlcp and GND.
Note: Leave the "NC" terminals open and do not connect them to GND.

Application circuit example



Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Light input window

If dust or dirt gets on the light input window, it will show up as black blemishes on the image. When cleaning, avoid rubbing the window surface with dry cloth or dry cotton swab, since doing so may generate static electricity. Use soft cloth, paper or a cotton swab moistened with alcohol to wipe dust and dirt off the window surface. Then blow compressed air onto the window surface so that no spot or stain remains.

(3) Soldering

To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

(4) Reflow soldering

Soldering conditions may differ depending on the board size, reflow furnace, etc. Check the conditions before soldering. A sudden temperature rise and fall may be the cause of trouble, so make sure that the temperature change is within 4 °C per second.

The bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

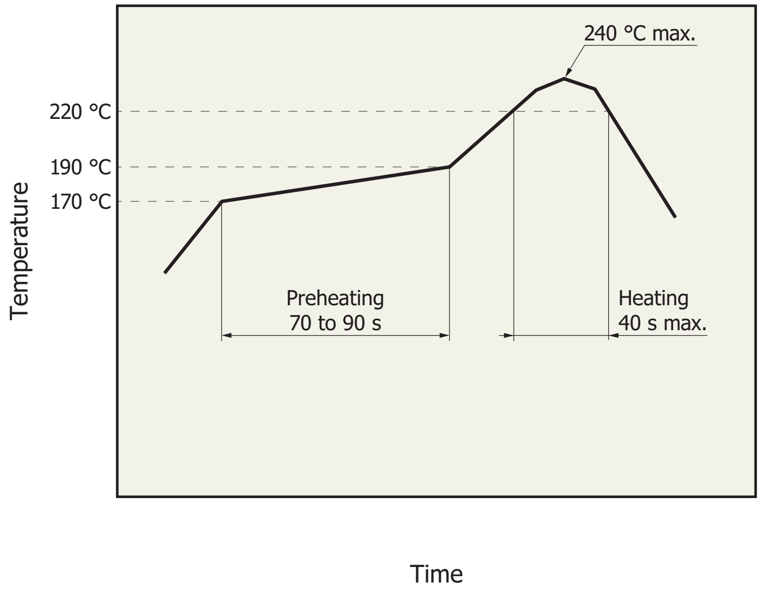
(5) Operating and storage environments

Always observe the rated temperature range when handling the device. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

(6) UV exposure

This device is designed to suppress performance deterioration due to UV exposure. Even so, avoid unnecessary UV exposure to the device. Also, be careful not to allow UV light to strike the cemented portion of the glass.

Actual data example of temperature profile measured with our hot-air reflow oven for product testing (leadfree product)



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Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
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