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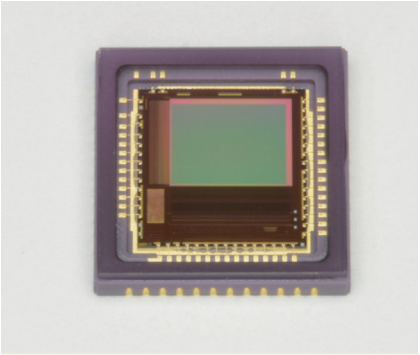
CMOS area image sensor



S13102

Near infrared high sensitivity, APS (active pixel sensor) type

The S13102 is an APS type CMOS area image sensor that has high sensitivity in the near infrared region. The pixel format is VGA (640 × 480 pixels). Imaging is possible at a maximum rate of 78 frames/s. It is an all-digital I/O type with built-in timing generator, bias generator, amplifier, and A/D converter. Rolling shutter readout or global shutter readout can be selected.

Features

- **Pixel size: 7.4 × 7.4 µm**
- **Number of pixels: 640 × 480 (VGA)**
- **Rolling/global shutter readout**
- **Readout noise: 5e⁻ rms (rolling shutter, at 8 times column amplifier gain)**
- **Single 3.3 V power supply operation**
- **SPI communication function (partial readout, gain switching, frame start mode selection, etc.)**
- **Partial readout function**

Applications

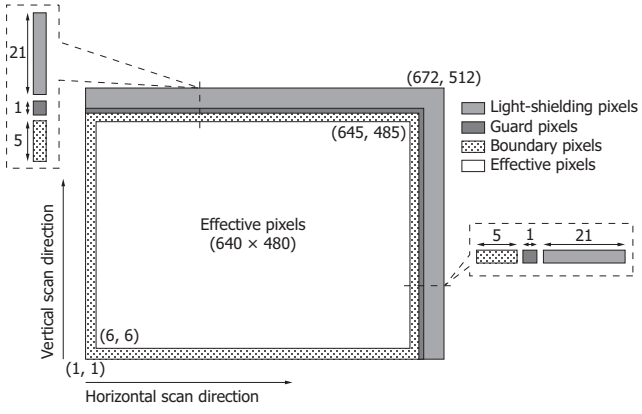
- **Near infrared laser beam detection (position detection, pattern recognition)**
- **Near infrared image detection (wafer transmission image, vein authentication, etc.)**

Structure

Parameter	Specification	Unit
Image size (H × V)	4.736 × 3.552	mm
Pixel size	7.4 × 7.4	µm
Pixel pitch	7.4	µm
Total number of pixels (H × V)	672 × 512	pixels
Number of effective pixels (H × V)	640 × 480	pixels
Boundary pixels*1	5 columns enclosing the effective pixel region	-
Guard pixels*2	Column 651 and row 491	
Light-shielding pixels*3	Columns 652 to 672 and rows 492 to 512	
Package	Ceramic	-
Window material	Borosilicate glass	-

*1: Same pixels as the effective pixels
*2: Pixels with a fixed photodiode potential
*3: Pixels whose photodiodes are shielded with metal

Pixel layout



KMPDC0598EA

Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Condition	Value	Unit
Supply voltage	Analog terminal	Vdd(A)		-0.3 to +3.9	V
	Digital terminal	Vdd(D)		-0.3 to +3.9	V
Digital input signal terminal voltage*4		Vi		-0.3 to +3.9	V
Vref_cp1 terminal voltage		Vref_cp1		-0.3 to +6.5	V
Vref_cp2 terminal voltage		Vref_cp2		-2.0 to +0.3	V
Operating temperature		Topr	No dew condensation*5	-40 to +85	°C
Storage temperature		Tstg	No dew condensation*5	-40 to +85	°C
Reflow soldering conditions*6 *7		Tsol		Peak temperature 260 °C, three times (see P.9)	-

*4: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_RESET, MST
*5: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*6: JEDEC level 3
*7: If the microlenses formed on the photosensitive area are exposed to high temperatures such as from reflow, the sensitivity in the 600 nm and lower spectral range may degrade. The higher the temperature or the longer the exposure, the greater the degree of degradation. As such, apply reflow for a short period of time, and avoid extraneous thermal load.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog terminal	Vdd(A)	3.0	3.3	3.6	V
	Digital terminal	Vdd(D)	3.0	Vdd (A)	3.6	V
Digital input terminal voltage*8	High level	Vi(H)	Vdd(D) - 0.25	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vi(L)	0	-	0.25	

*8: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_RESET, MST

Electrical characteristics

■ Digital input signal [Ta=25 °C, recommended operating conditions Typ. (P.2), unless otherwise noted]*8

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency	f(MCLK)	10	-	30	MHz
Master clock pulse duty cycle	D(MCLK)	45	50	55	%
Rise time*9	tr(sigi)	-	5	7	ns
Fall time*9	tf(sigi)	-	5	7	ns

*8: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_RESET, MST
*9: Time for the input voltage to rise or fall between 10% and 90%

■ Digital output signal [Ta=25 °C, recommended operating conditions Typ. (P.2), unless otherwise noted]*10

Parameter		Symbol	Min.	Typ.	Max.	Unit
Video data rate		VR		f(MCLK)		Hz
Digital output voltage	High	Vsigo(H)	Vdd(D) - 0.25	Vdd(D)	-	V
	Low	Vsigo(L)	-	0	0.25	V
Rise time*11		tr(sigo)	-	10	12	ns
Fall time*11		tf(sigo)	-	10	12	ns

*10: Pclk, Vsync, Hsync, Dout, SPI_MISO
*11: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor is attached to the output terminal

■ Current consumption [Ta=25 °C, recommended operating conditions Typ. (P.2), digital input signal Typ. (P.2), unless otherwise noted]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Analog terminal*12	I1	-	70	110	mA
Digital terminal*12	I2	-	50	80	

*12: Dark state, master clock pulse frequency=30 MHz, frame rate=78.6 frames/s, load capacitance of each output terminal=5 pF

Electrical characteristics of A/D converter [Ta=25 °C, recommended operating conditions Typ. (P.2), digital input signal Typ. (P.2), unless otherwise noted]

Parameter	Symbol	Specification	Unit
Resolution	RESO	12	bit
Conversion time	tCON	1/f(MCLK)	s
Conversion voltage range	-	0 to 2	V

Electrical and optical characteristics [Ta=25 °C, recommended operating conditions Typ., digital input signal Typ., MCLK=30 MHz, gain: default, offset: default, rolling shutter, integration time=14 ms, unless otherwise noted]

■ Common to all modes

Parameter			Symbol	Min.	Typ.	Max.	Unit
Spectral response range			λ		400 to 1100		nm
Peak sensitivity wavelength			λp	-	700	-	nm
Photoresponse nonuniformity*13			PRNU	-	-	4	%
Defective pixels	Point defect	White spot*14	WS	-	-	10	pixels
		Black spot*15	BS	-	-	10	pixels
	Cluster defect*16		ClsD	-	-	0	pcs

*13: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the photosensitive area is uniformly illuminated by white light which is approx. 50% of the saturation level. PRNU is calculated using the pixels excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels, and is defined as follows:
PRNU = (ΔX/X) × 100 [%], ΔX: standard deviation, X: average output of all pixels
*14: Pixels whose dark output exceeds 1500 DN/s at gain=2 in rolling shutter mode (excluding boundary pixels and guard pixels)
*15: Pixels whose output value is 50% or less than that of adjacent pixels in a condition in which uniform light equivalent to the mid-point of saturated output is applied (excluding boundary pixels, guard pixels, and light-shielding pixels)
*16: Point defect spanning two or more consecutive pixels

■ Global shutter mode

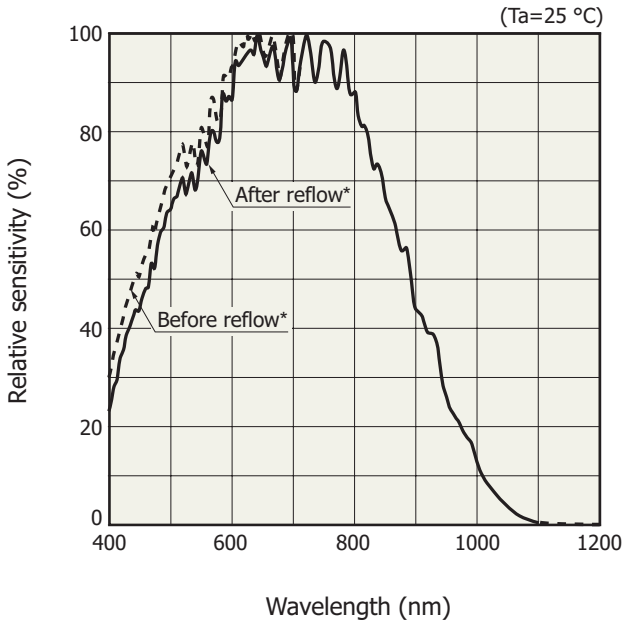
Parameter	Symbol	Min.	Typ.	Max.	Unit
Offset output*17	Vo	200	700	1200	DN
Offset variation*18	DSNU	-	15	100	DN rms
Dark output*17	DS	-	5	20	DN/s
Saturation exposure*19	Lsat	-	0.32	-	lx·s
Photosensitivity*19	Sw	4400	5600	-	DN/lx·s
Saturation output*20	Vsat	1600	2300	-	DN
Random noise*17	RN	-	2.3	4	DN rms
Dynamic range*21	DR	56	60	-	dB
Conversion factor	-	-	37	-	μV/e^-
	-	-	0.074	-	DN/e^-

■ Rolling shutter mode

Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset output*17	Vo	1	200	700	1200	DN
		2	200	700	1200	
		8	200	700	1200	
Offset variation*18	DSNU	1	-	3	10	DN rms
		2	-	3	15	
		8	-	3	15	
Dark output*17	DS	1	-	5	20	DN/s
		2	-	10	40	
		8	-	40	160	
Saturation exposure*19	Lsat	1	-	0.32	-	lx·s
		2	-	0.16	-	
		8	-	0.04	-	
Photosensitivity*19	Sw	1	4400	5600	-	DN/lx·s
		2	8900	11200	-	
		8	33900	42500	-	
Saturation output*20	Vsat	1	1600	2300	-	DN
		2	2500	3500	-	
		8	3000	3500	-	
Random noise*17	RN	1	-	1	2	DN rms
		2	-	1.5	4	
		8	-	2.8	4	
Dynamic range*21	DR	1	58	67	-	dB
		2	56	67	-	
		8	57	62	-	
Conversion factor		1	-	37	-	μV/e^-
			-	0.074	-	DN/e^-
		2	-	74	-	μV/e^-
			-	0.148	-	DN/e^-
		8	-	280	-	μV/e^-
			-	0.56	-	DN/e^-

*17: Average output of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*18: Standard deviation of output of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*19: λ=555 nm
*20: Average of values without the offset output of pixels in a condition in which light equivalent to twice the saturation exposure is applied (excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels).
*21: Ratio of saturation output to random noise
Note, DN (digital number): unit of A/D converter output

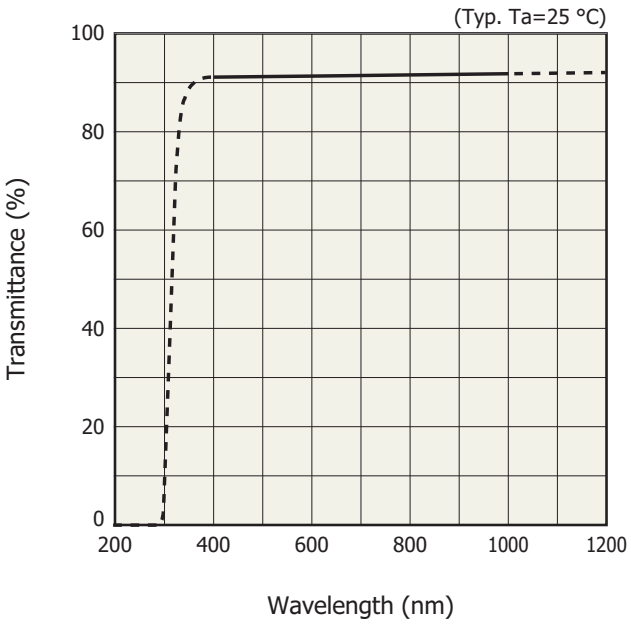
Spectral response (typical example)



* Executed after using the recommended temperature profile for reflow soldering (P9: preheat 100 s, soldering 100 s, peak temperature 260 °C).

KMPDB0488ED

Spectral transmittance characteristics of window material



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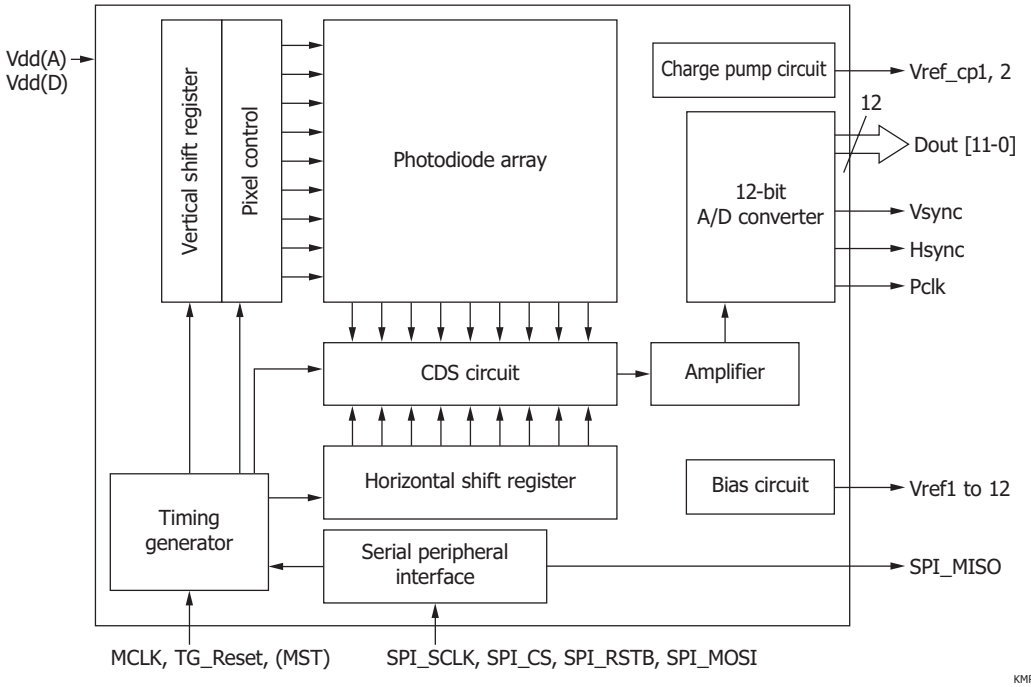
Block diagram



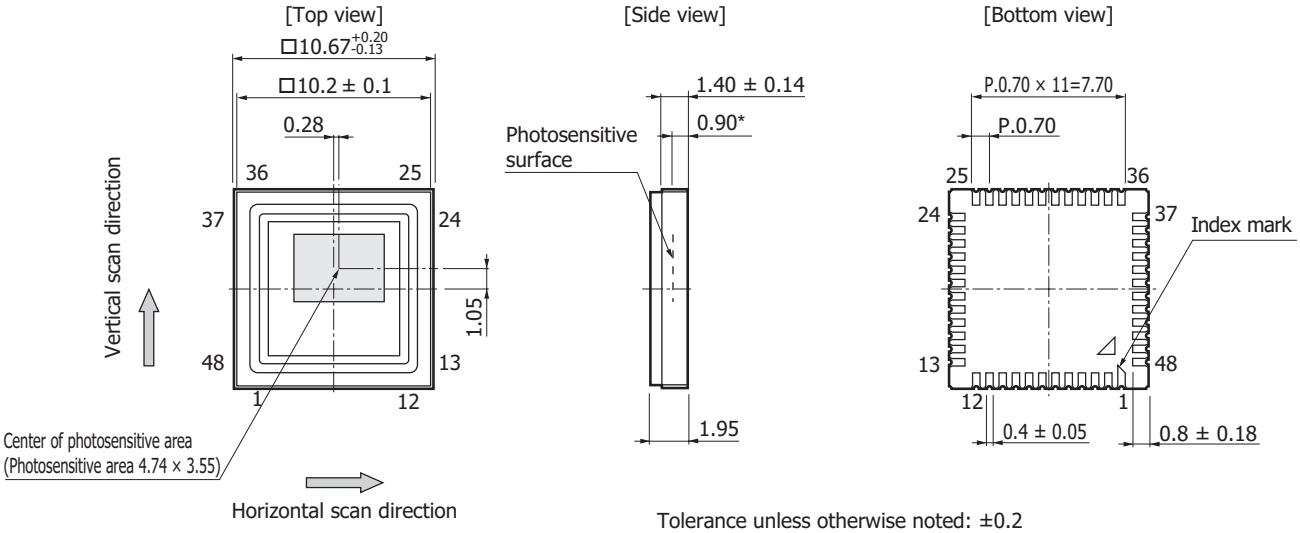
KMPDC0565EC

Setup using the SPI and the like

The following parameters can be set using the SPI (serial peripheral interface). The integration time and blanking period in external start mode is set using MST (external input signals).

Parameter	Mode and explanation	
Shutter mode (default: rolling shutter mode)	Rolling shutter mode	Rolling shutter mode is advantageous in that readout noise is small because readout is performed through the CDS circuit. However, the disadvantage is that the integration start/end timing is different for each row.
	Global shutter mode	Global shutter mode is advantageous in that the integration start/end timing is the same for all pixels. However, the disadvantage is that the readout noise is large because a CDS circuit is not used.
Frame start mode (default: internal start pulse mode)	Internal start pulse mode	Readout starts automatically when the power is turned on. The frame period is determined by the number of readout rows and columns and the blanking period.
	External start pulse mode	Readout starts when the rising edge of MST is detected. MST is also used to control the integration time. The low-level period of MST is roughly the integration time.
Integration time	Internal start pulse mode	Integration time is set using SPI.
	External start pulse mode	Integration time is set using MST.
Blanking period	Internal start pulse mode	Blanking period can be set for 0 to 65535 rows using SPI.
	External start pulse mode	Blanking period is from the end of a readout to the rising edge of the next MST.
Readout region	The readout region can be set at the pixel level. A single readout region can be set in each frame.	
Output gain (rolling shutter mode only)	The gain can be set to 1 time, 2 times, or 8 times.	
Output offset	The output offset value can be adjusted. The default output level is approximately 500 DN.	

Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.2
Angle accuracy of effective pixels: ±3.15°
Weight: 0.5 g
* Distance from package bottom to photosensitive surface

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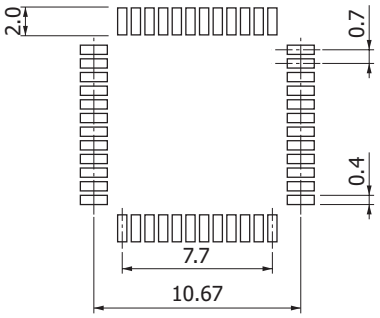
Recommended land pattern (unit: mm)



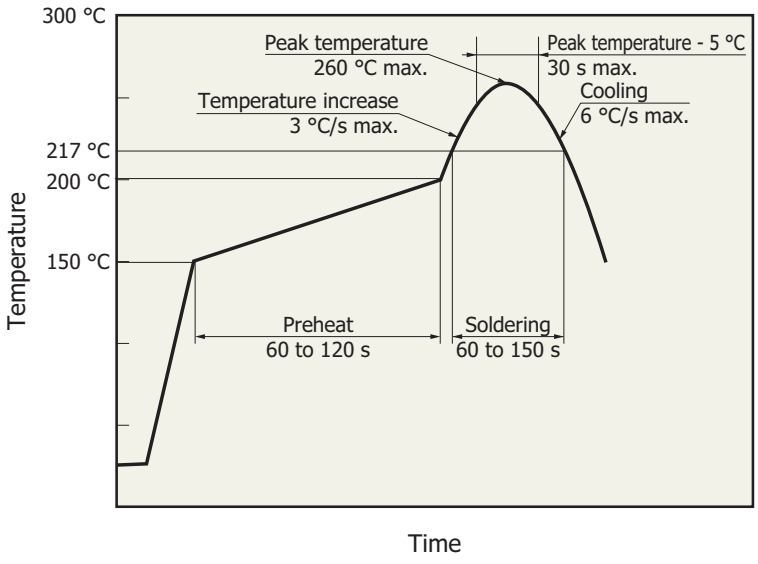
KMPDC0528EA

Pin connections

Pin no.	Symbol	Description	I/O
1	Dout0	Video output signal (LSB)	O
2	Dout1	Video output signal	O
3	Dout2	Video output signal	O
4	Dout3	Video output signal	O
5	Dout4	Video output signal	O
6	Dout5	Video output signal	O
7	Dout6	Video output signal	O
8	Dout7	Video output signal	O
9	Dout8	Video output signal	O
10	Dout9	Video output signal	O
11	Dout10	Video output signal	O
12	Dout11	Video output signal (MSB)	O
13	Vdd(A)	Analog supply voltage*22 *24	I
14	GND	Ground	I
15	Vref1	Bias voltage for A/D converter*22	O
16	Vref2	Bias voltage for A/D converter*22	O
17	Vref3	Bias voltage for A/D converter*22	O
18	Vref4	Bias voltage for A/D converter*22	O
19	Vref5	Bias voltage for A/D converter*22	O
20	Vdd(A)	Analog supply voltage*22 *24	I
21	GND	Ground	I
22	Vref6	Bias voltage for amplifier*22	O
23	Vref7	Bias voltage for amplifier*22	O
24	Vref8	Bias voltage for amplifier*22	O
25	Vref9	Bias voltage for CDS*22 *23	O
26	Vref10	Bias voltage for amplifier*22 *23	O
27	Vref11	Bias voltage for amplifier*22 *23	O
28	Vref12	Bias voltage for amplifier*22 *23	O
29	Vdd(A)	Analog supply voltage*22 *24	I
30	Vdd(D)	Digital supply voltage*22 *24	I
31	Vdd(A)	Analog supply voltage*22 *24	I
32	Vref_cp1	Bias voltage for charge pump circuit*22 *23	I
33	GND	Ground	I
34	Vref_cp2	Bias voltage for charge pump circuit*22 *23	I
35	MST	Master start clock signal	I
36	SPI_MISO	SPI output signal	O
37	SPI_CS	SPI selection signal	I
38	SPI_SCLK	SPI clock signal	I
39	SPI_MOSI	SPI input signal	I
40	SPI_RSTB	SPI reset signal	I
41	TG_RESET	Reset signal	I
42	MCLK	Master clock signal	I
43	Vsync	Frame sync signal	O
44	Hsync	Line sync signal	O
45	Pclk	Pixel output sync signal	O
46	Vdd(D)	Digital supply voltage*22 *24	I
47	GND	Ground	I
48	Vdd(D)	Digital supply voltage*22 *24	I

*22: To reduce noise, insert a capacitor around 1 µF between each terminal and GND.
*23: A terminal for monitoring the bias voltage generated inside the chip
*24: Apply voltage to all supply voltage terminals.

Recommended temperature profile for reflow soldering (typical example)



· This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 168 hours.
· The effect that the product is subject to during reflow soldering varies depending on the circuit board and reflow oven that are used. Before actual reflow soldering, check for any problems by testing out the reflow soldering methods in advance.

Recommended baking condition

See Precautions (surface mount type products).

Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.

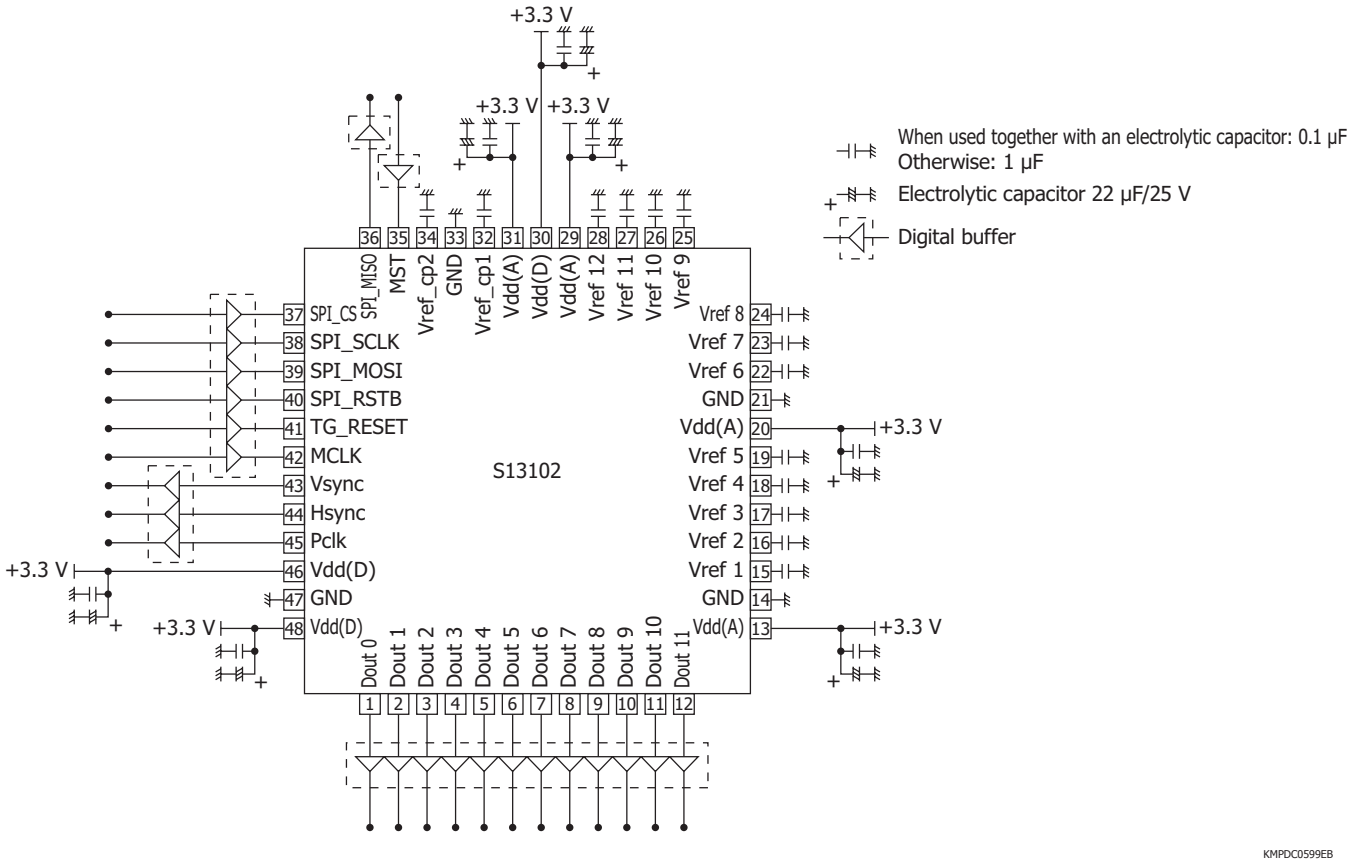
(2) Light input window
If dust or stain adheres to the surface of the light input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth or a cotton swab moistened with alcohol to wipe dust and stain off the window surface. Then blow compressed air onto the window surface so that no dust or stain remains.

(3) Soldering
To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

(4) Reflow soldering
Soldering conditions vary depending on the size of the circuit board, reflow oven, and the like. Check the conditions advance before soldering. Note that the bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

(5) UV light irradiation
This product is not designed to resist characteristic deterioration under UV light irradiation. Do not apply UV light to it.

Connection circuit example



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Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

· Disclaimer
· Image sensors
· Surface mount type products

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