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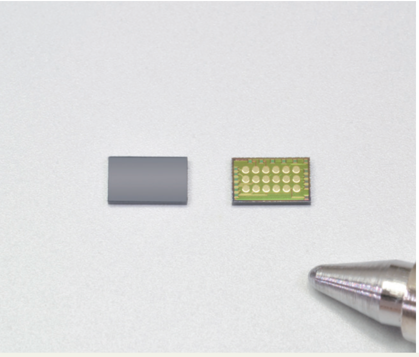
NEW

Distance linear image sensor

S15452-01WT



Back-thinned type, measures the distance to an object by TOF method

The distance image sensor is designed to measure the distance to an object by TOF (time-of-flight) method. When used in combination with a pulse modulated light source, this sensor outputs phase difference information on the timing that the light is emitted and received. Distance data can be obtained by performing calculation on the output signal with an external signal processing circuit or on a PC. We provide an evaluation kit for this product. Contact us for detailed information.

Features

- **High sensitivity in the near infrared region**
- **Improved tolerance to background light**
- **Compact wafer level package (WLP) type**

Applications

- **Obstacle detection (self-driving, robots, etc.)**
- **Security (intrusion detection, etc.)**
- **Shape recognition (logistics, robots, etc.)**
- **Motion capture**
- **Touchless operation**

Structure

Parameter	Specification	Unit
Image size	1.28 × 0.05	mm
Pixel pitch	20	μm
Pixel height	50	μm
Number of pixels	80	pixels
Number of effective pixels	64	pixels
Package	WLP	-

Note: This product is not hermetically sealed.

Absolute maximum ratings

Parameter		Symbol	Condition	Value	Unit
Analog supply voltage		Vdd(A)	Ta=25 °C	-0.3 to +4.2	V
Digital supply voltage		Vdd(D)	Ta=25 °C	-0.3 to +4.2	V
Analog input terminal voltage	Pixel amplifier	Vsf	Ta=25 °C	-0.3 to Vdd(A) + 0.3	V
	Pixel reset	Vr			
	Photosensitive area	Vpg			
Digital input terminal voltage	Pixel reset pulse	pix_reset	Ta=25 °C	-0.3 to Vdd(D) + 0.3	V
	Signal sampling pulse	phis			
	Master clock pulse	mclk			
	Signal readout trigger pulse	trig			
	Output signal sync pulse	dclk			
Charge transfer clock pulse voltage		VTX1, VTX2, VTX3	Ta=25 °C	-0.3 to Vdd(A) + 0.3	V
Operating temperature		Topr	No dew condensation*1	-25 to +85	°C
Storage temperature		Tstg	No dew condensation*1	-40 to +85	°C
Soldering temperature*2		Tsol		245 (twice)	°C

*1: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*2: Reflow soldering, IPC/JEDEC J-STD-020 MSL 2, see P.9
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Analog supply voltage		Vdd(A)	3.2	3.3	3.4	V
Digital supply voltage		Vdd(D)	3.2	3.3	3.4	V
Bias voltage	Pixel amplifier	Vsf	-	Vdd(A)	-	V
	Pixel reset	Vr	2.5	2.6	2.7	V
	Photosensitive area	Vpg	0.6	0.8	1.0	V
Pixel reset pulse voltage	High level	pix_reset	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Signal sampling pulse voltage	High level	phis	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Master clock pulse voltage	High level	mclk	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Signal readout trigger pulse voltage	High level	trig	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Output signal sync pulse voltage	High level	dclk	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	

Electric characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

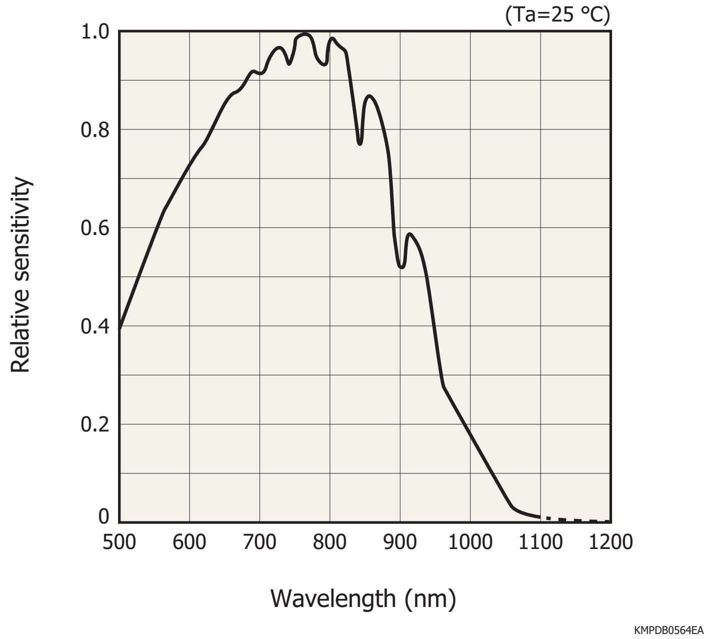
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(mclk)		1 M	-	5 M	Hz
Data rate	DR		-	f(mclk)	-	Hz
Current consumption	Ic	Dark state	-	6	-	mA

Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, Vsf=3.3 V, Vr=2.6 V, MCLK=5 MHz]

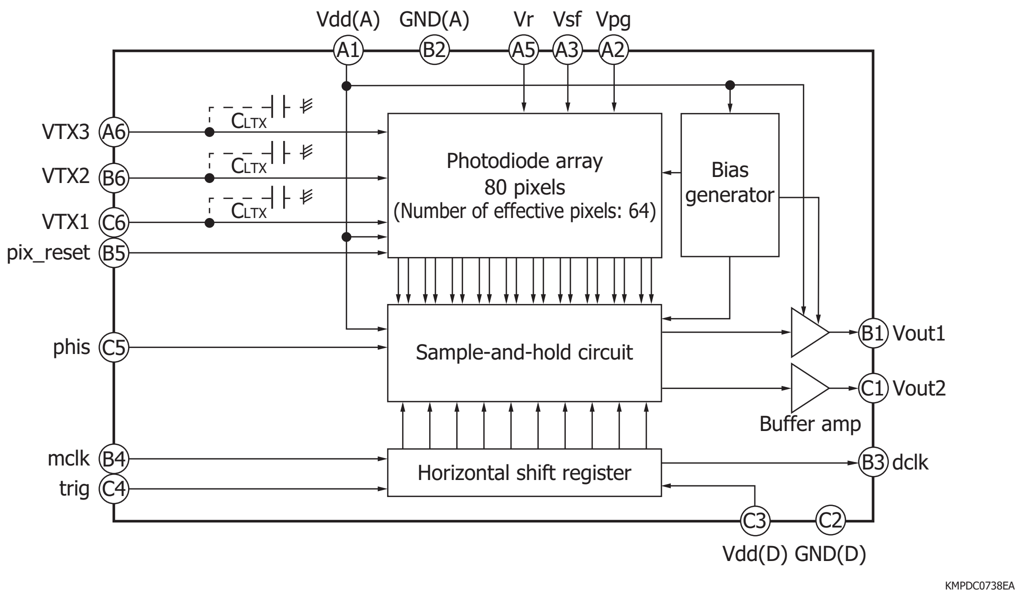
Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ		500 to 1100		nm
Peak sensitivity wavelength	λp	-	800	-	nm
Photosensitivity*3	S	-	1.4×10^{12}	-	$V/W \cdot s \cdot m^2$
Dark output	Vd	-	2.8	5	V/s
Random noise	RN	-	0.5	1	mV rms
Dark output voltage*4	Vor	-	2.7	-	V
Sensitivity ratio*5	SR	0.7	-	1.43	-
Photoresponse nonuniformity*6	PRNU	-	-	±10	%

*3: Monochromatic wavelength light source (λ=805 nm)
*4: Output value right after reset in dark state
*5: Output ratio of Vout1 (VTX1=1.8 V, VTX2=VTX3=0 V) to Vout2 (VTX2=1.8 V, VTX1=VTX3=0 V)
*6: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 64 pixels excluding 8 pixels each at both ends, and is defined as follows.
$PRNU = \Delta X / X \times 100$ [%]
X: average of the output of all pixel, ΔX: difference between the maximum or minimum output and X

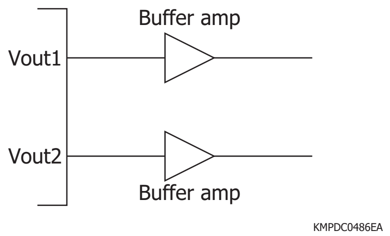
Spectral response (typical example)



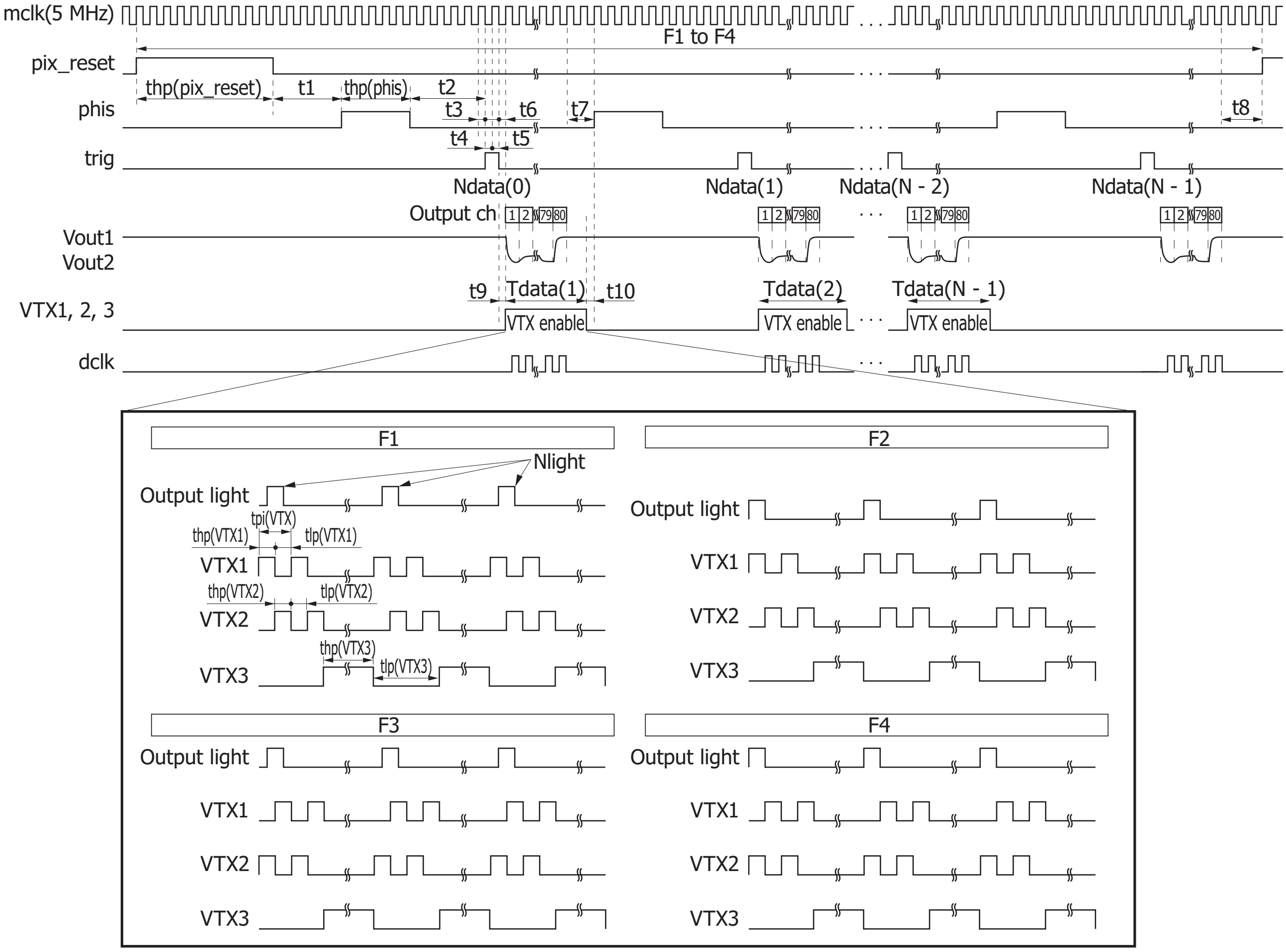
Block diagram



Basic connection example



Timing chart



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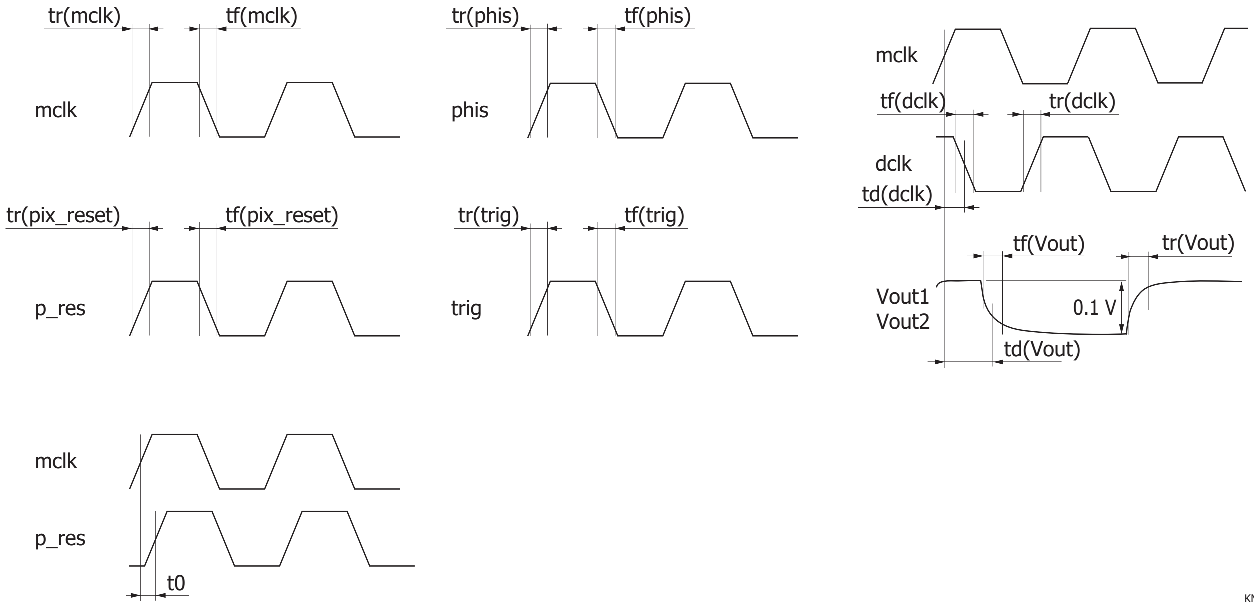

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Calculation method of frame rate

Frame rate=1/4 of subframe time

- If the integration time is longer than the readout time
  Time per subframe=Integration time × (Non-destructive readout count - 1) + Readout time

- If the integration time is shorter than the readout time
  Time per subframe=Readout time × Non-destructive readout time

Note: The integration time setting needs to be changed depending on the required distance accuracy and usage environment factors such as background light.

[Readout time calculation]

$$\text{Readout time} = \frac{1}{\text{Clock pulse frequency}} \times \text{Number of horizontal pixels}$$

$$= \text{Time per clock (Readout time per pixel)} \times \text{Number of horizontal pixels}$$

· Calculation example (clock pulse frequency=5 MHz, number of horizontal pixels=80)

$$\text{Readout time} = \frac{1}{5 \times 10^6\ [\text{Hz}]} \times 80$$

$$= 200\ [\text{ns}] \times 80$$

$$= 0.016\ [\text{ms}]$$

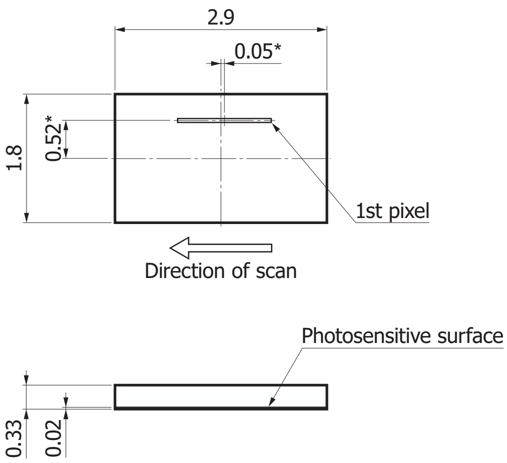
Parameter		Symbol	Min.	Typ.	Max.	Unit
Master clock pulse duty ratio		-	45	50	55	%
Master clock pulse rise and fall times[*7]		tr(mclk), tf(mclk)	0	-	20	ns
Pixel reset pulse high period		thp(pix_reset)	10	-	-	μs
Pixel reset pulse rise and fall times[*7]		tr(pix_reset), tf(pix_reset)	0	-	20	ns
Signal sampling pulse high period		thp(phis)	1	-	-	μs
Signal sampling pulse rise and fall times[*7]		tr(phis), tf(phis)	0	-	20	ns
Signal readout trigger pulse rise and fall times[*7]		tr(trig), tf(trig)	0	-	20	ns
Time from rising edge of master clock pulse to rising edge of pixel reset pulse		t0	0	-	-	ns
Time from falling edge of pixel reset pulse to rising edge of signal sampling pulse		t1	1	-	-	μs
Time from falling edge of signal sampling pulse to rising edge of signal readout trigger pulse		t2	1.2	-	-	μs
Time from rising edge of master clock pulse to rising edge of signal readout trigger pulse		t3	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of signal readout trigger pulse to rising edge of master clock pulse		t4	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of master clock pulse to falling edge of signal readout trigger pulse		t5	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of signal readout trigger pulse to rising edge of master clock pulse		t6	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of master clock pulse (after reading signals from all pixels) to rising edge of output signal sampling pulse		t7	1/f(mclk)	-	-	s
Time from rising edge of master clock pulse (after reading signals from all pixels) to rising edge of pixel reset pulse		t8	1/f(mclk)	-	-	s
Time from rising edge of master clock pulse to falling edge of output signal sync pulse[*8]		td(dclk)	-	7	-	ns
Output signal sync pulse rise time[*7 *8]		tr(dclk)	-	12	-	ns
Output signal sync pulse fall time[*7 *8]		tf(dclk)	-	8	-	ns
Settling rise time of output signal 1, 2[*7 *8 *9]		tr(Vout)	-	20	-	ns
Settling fall time of output signal 1, 2[*7 *8 *9]		tf(Vout)	-	20	-	ns
Time from rising edge of master clock pulse to output signal 1, 2 (output 50%)[*8]		td(Vout)	-	18	-	ns
Charge transfer clock pulse cycle		tpi(VTX)	60	-	-	ns
Charge transfer clock pulse (VTX1)	High period	thp(VTX1)	30	-	-	ns
	Low period	tlp(VTX1)	-	tpi(VTX) thp(VTX2) thp(VTX3)	-	
Charge transfer clock pulse (VTX2)	High period	thp(VTX2)	30	-	-	ns
	Low period	tlp(VTX2)	-	tpi(VTX) thp(VTX1) thp(VTX3)	-	
Charge transfer clock pulse (VTX3)	High period	thp(VTX3)	0	-	-	ns
	Low period	tlp(VTX3)	-	tpi(VTX) thp(VTX1) thp(VTX2)	-	
Charge transfer clock pulse voltage rise and fall times[*7]		tr(VTX), tf(VTX)	-	3	-	ns
Charge transfer clock Pulse voltage	High level	VTX1, VTX2, VTX3	1.6	1.8	2.0	V
	Low level		-	0	-	V
Time from falling edge of signal readout trigger pulse to start of VTX drive		t9	1/f(mclk)	-	-	s
Time from end of VTX drive to rising edge of output sync pulse		t10	1/f(mclk)	-	-	s

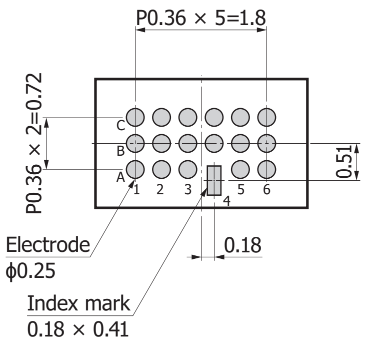
*7: 10 to 90%
*8: Load capacitance C_L=3 pF
*9: Output voltage=0.1 V

Input terminal capacitance (Ta=25 °C, Vdd=3.3 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Charge transfer clock pulse internal load capacitance	CLTX	-	10	-	pF

Dimensional outline (unit: mm)





Tolerance unless otherwise noted: ±0.1
Au electrode
* Distance from package center to photosensitive area center

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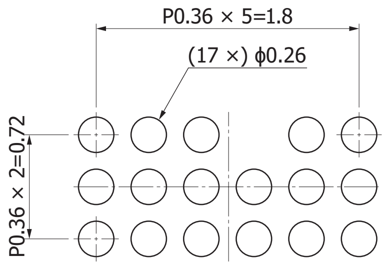
Recommended land pattern (unit: mm)



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Pin connections

Pin no.	Symbol	I/O	Description
A1	Vdd(A)	I	Analog supply voltage
B1	Vout1	O	Output signal 1
C1	Vout2	O	Output signal 2
A2	Vpg	I	Photosensitive area bias voltage
B2	GND(A)	I	Ground
C2	GND(D)	I	Ground
A3	Vsf	I	Pixel amplifier drain voltage
B3	dclk	O	Output data sample clock
C3	Vdd(D)	I	Digital supply voltage
A4	NC	-	No connection
B4	mclk	I	Master clock input signal
C4	trig	I	Signal readout trigger signal (reset and signal level)
A5	Vr	I	Pixel reset voltage
B5	pix_reset	I	Pixel reset pulse
C5	phis	I	Signal sampling signal (level determined on the falling edge)
A6	VTX3	I	Charge transfer clock 3 (for OFD)
B6	VTX2	I	Charge transfer clock 2
C6	VTX1	I	Charge transfer clock 1

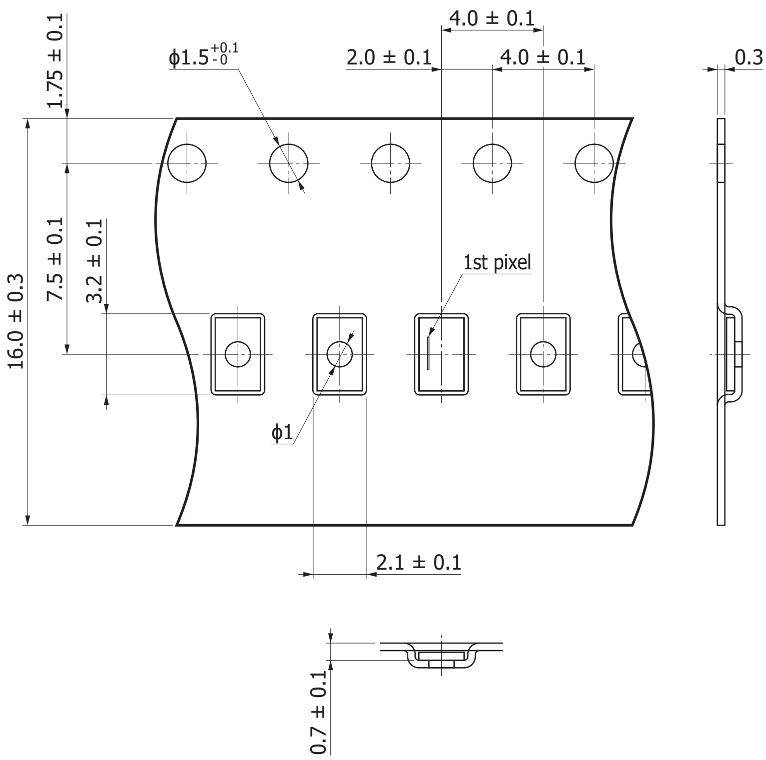
Note: Leave the NC terminals open.
Connect an impedance converting buffer amplifier to Vout1 and Vout2 terminals so as to minimize the current flow.

Reel packing specifications

■ Reel (conforms to JEITA ET-7200)

Outer diameter	Hub diameter	Tape width	Material	Electrostatic characteristics
ϕ180 mm	ϕ60 mm	16 mm	PS	Conductive

■ Embossed tape (unit: mm, material: PS, conductive)



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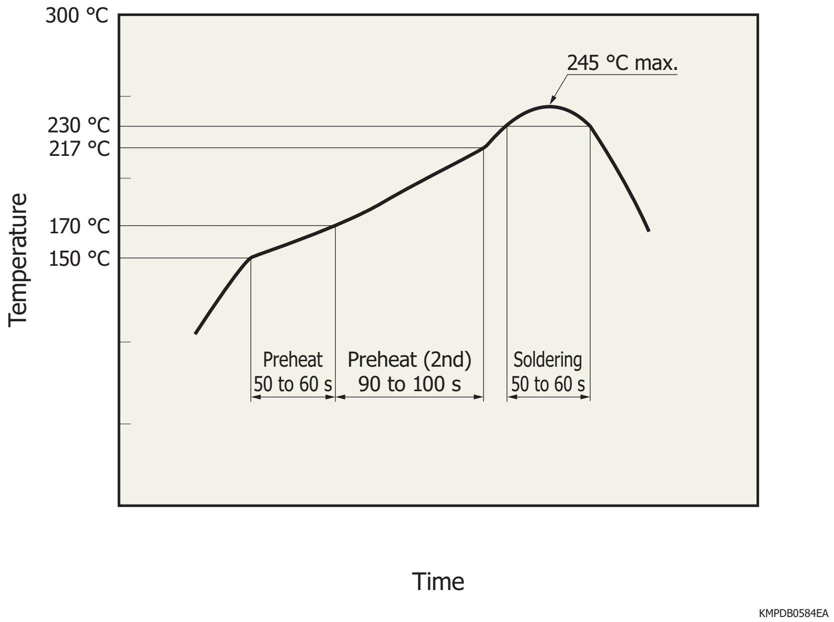
■ Packing quantity

500 pcs/reel

■ Packing state

Reel and desiccant in moisture-proof packaging (vacuum-sealed)

Recommended soldering conditions



· This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 1 year.
· The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. When you set reflow soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.
· In order to improve reliability, we recommend that you use underfill resin to fill the gap between the element and the board, after reflow soldering.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Surface mount type products

■ Technical information
· Distance image sensors (Back-thinned type) S15452/S15453/S15454-01WT

Evaluation kit for distance linear image sensor C15356

An evaluation kit [70 mm (H) × 55 mm (V)] is available for the S15452-01WT distance linear image sensor (with the S15452-01WT). Contact us for detailed information.

Information described in this material is current as of July 2020.
Product specifications are subject to change without prior notice due to improvements or other reasons. This document has been carefully prepared and the information contained is believed to be accurate. In rare cases, however, there may be inaccuracies such as text errors. Before using these products, always contact us for the delivery specification sheet to check the latest specifications.
The product warranty is valid for one year after delivery and is limited to product repair or replacement for defects discovered and reported to us within that one year period. However, even if within the warranty period we accept absolutely no liability for any loss caused by natural disasters or improper product use.
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Cat. No. KMPD1218E03 Jul. 2020 DN