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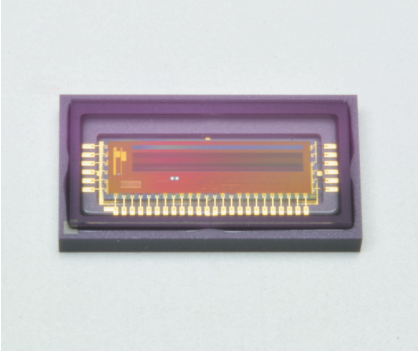
NEW

CMOS linear image sensor



S15611

40 MHz operation, digital output

The S15611 is a CMOS linear image sensor that has achieved a readout speed of 40 MHz max. and a line rate of 34 kHz max. The image sensor has a timing generator, bias generator, 12-bit A/D converter, and is easy to handle because of its digital I/O.

Features

- **Pixel size: 7 × 200 µm**
- **1024 pixels**
- **Effective photosensitive area length: 7.168 mm**
- **High-speed readout: 40 MHz max.**
- **Simultaneous integration of all pixels**
- **With variable integration time function (electronic shutter function)**
- **Single 3.3 V supply voltage operation**
- **SPI communication function (partial readout, offset adjustment)**
- **Built-in 12-bit A/D converter**

Applications

- **Encoders**
- **Position detection**
- **Machine vision**

Structure

Parameter	Specification	Unit
Number of pixels	1024	-
Pixel pitch	7	µm
Pixel height	200	µm
Effective photosensitive area length	7.168	mm
Package	Ceramic	-
Window material	Borosilicate glass	-

Absolute maximum ratings

Parameter		Symbol	Condition	Value	Unit
Supply voltage	Analog terminal	Vdd(A)	Ta=25 °C	-0.3 to +3.9	V
	Digital terminal	Vdd(D)	Ta=25 °C	-0.3 to +3.9	
Digital input terminal voltage*1		Vi	Ta=25 °C	-0.3 to +3.9	V
Vref_cp1 terminal voltage		Vref_cp1	Ta=25 °C	-0.3 to +6.5	V
Vref_cp2 terminal voltage		Vref_cp2	Ta=25 °C	-2.0 to +0.3	V
Operating temperature		Topr	No dew condensation*2	-5 to +70	°C
Storage temperature		Tstg	No dew condensation*2	-10 to +70	°C
Soldering temperature*3		Tsol		260 (3 times)	°C

*1: MOSI, SCLK, CS, RSTB, MCLK, MST
*2: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*3: Reflow soldering, JEDEC J-STD-020 MSL 4, see P.12
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog terminal	Vdd(A)	3.15	3.3	3.6	V
	Digital terminal	Vdd(D)	3.15	3.3	3.6	
Digital input terminal voltage	High level	Vi(H)	3	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vi(L)	0	-	0.3	

Electrical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency		MCLK	5	-	40	MHz
Data rate		DR	-	f(MCLK)	-	MHz
Line rate*4		FR	-	-	34	kHz
Digital output voltage	High level	Vdo(H)	Vdd(D) - 0.25	Vdd(D)	-	V
	Low level	Vdo(L)	-	0	0.25	
Current consumption*5		Ic	-	160	200	mA

*4: When all pixels (1024 pixels) are read out
*5: f(MCLK)=40 MHz
Current consumption changes according to the master clock pulse frequency.

Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, f(MCLK)=40 MHz]

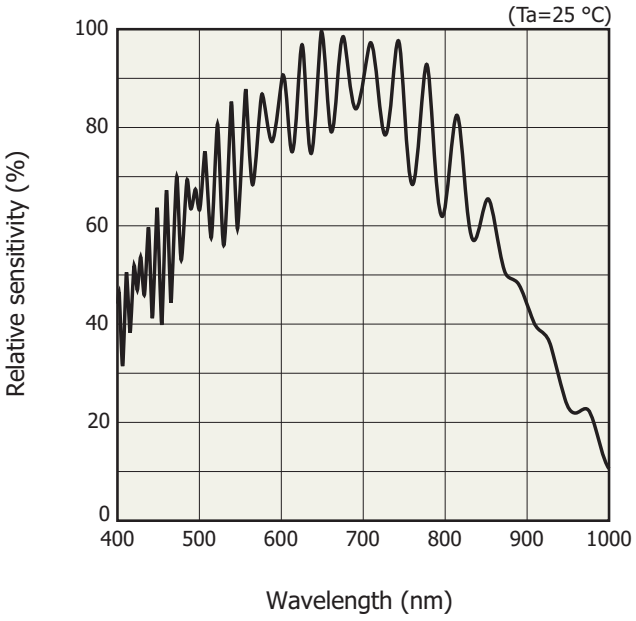
Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ		400 to 1000		nm
Peak sensitivity wavelength	λp	-	700	-	nm
Photosensitivity*6	Sw	-	1350	-	V/(lx·s)
		-	2765 k	-	DN/(lx·s)
Conversion efficiency	CE	-	40	-	μV/e⁻
Photoresponse nonuniformity*7	PRNU	-	±5	±10	%
Dark output*8	VD	-	1.2	12	mV
		-	2.5	25	DN
Saturation charge	Qsat	42	43	-	ke⁻
Saturation output	Vsat	1.47	1.71	-	V
		3000	3500	-	DN
Readout noise*9	Nread	-	0.63	1.9	mV rms
		-	1.3	3.9	DN rms
Dynamic range*10	Drange	-	2700	-	-
Output offset*11	Voffset	0.122	0.244	0.366	mV
		250	500	750	DN
Image lag*12	Lag	-	-	0.1	%

*6: 2856 K, tungsten lamp
*7: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 1018 pixels excluding the 3 pixels at both ends, and is defined as follows:
PRNU=ΔX/X × 100 [%]
X: average output of all pixels, ΔX: difference between the maximum or minimum output and X
*8: Ts=10 ms, difference from the offset output
*9: Dark state
*10: Vsat/Nread
*11: Initial value. The offset level can be changed through the SPI.
*12: If output of the previous frame exceeds the saturation output, it is the signal that remains in the next frame.

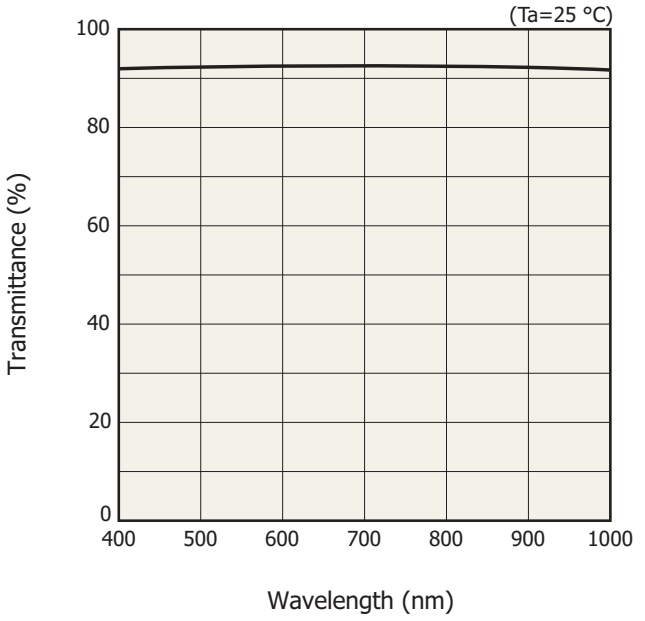
Electrical and optical characteristics [A/D converter, Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

Parameter	Symbol	Value	Unit
Resolution	RESO	12	bit
Conversion time	tCON	1/f(MCLK)	s
Conversion voltage range	-	0 to 2	V

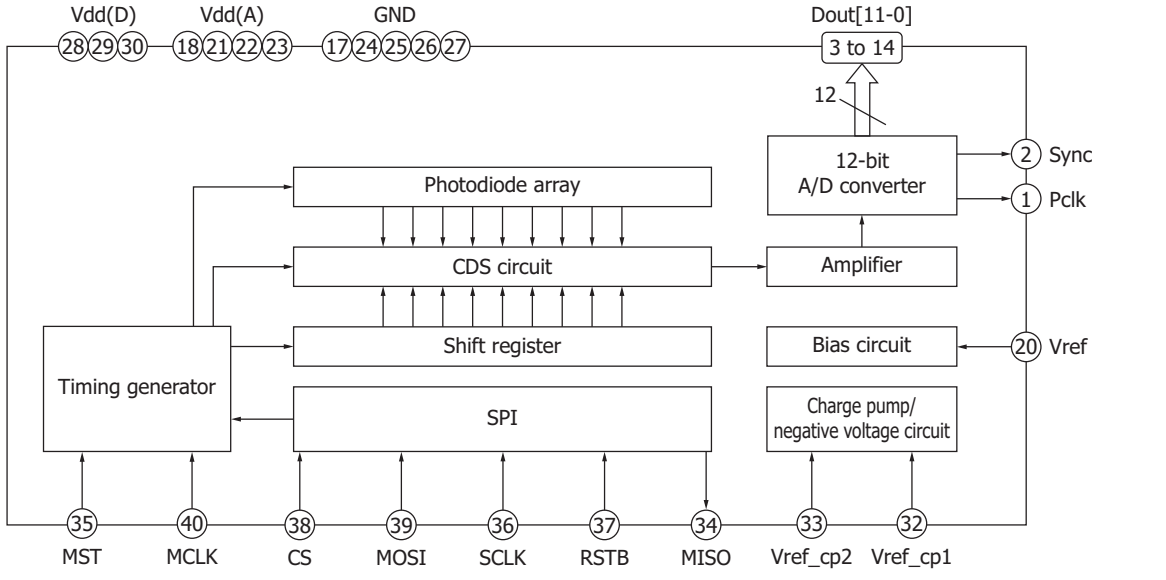
Spectral response (typical example)



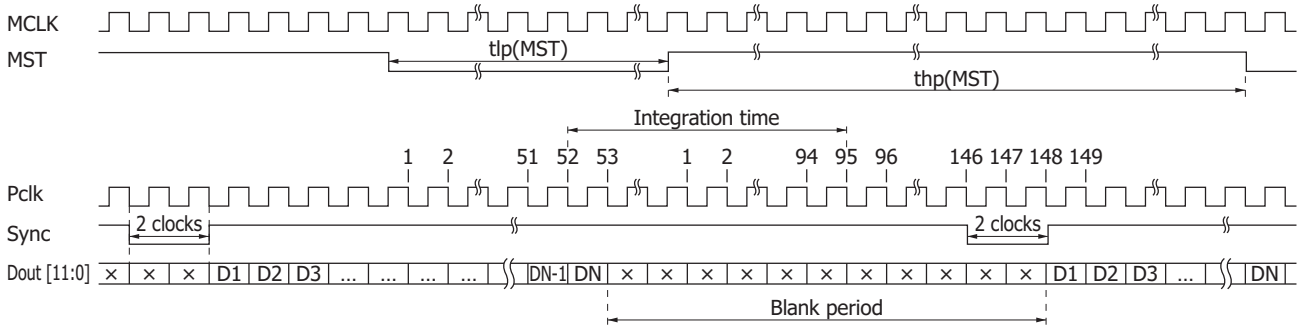
Spectral transmittance characteristics of window material (typical example)

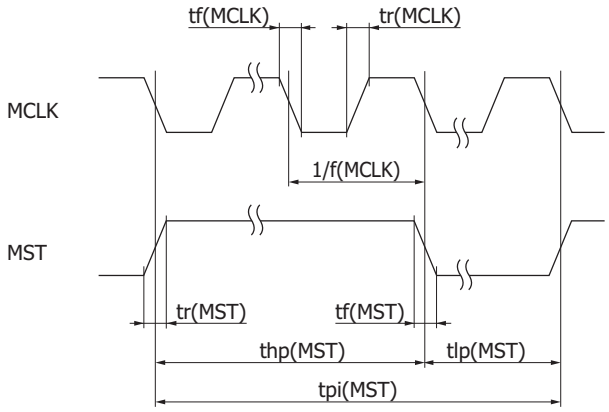


Block diagram



Timing chart





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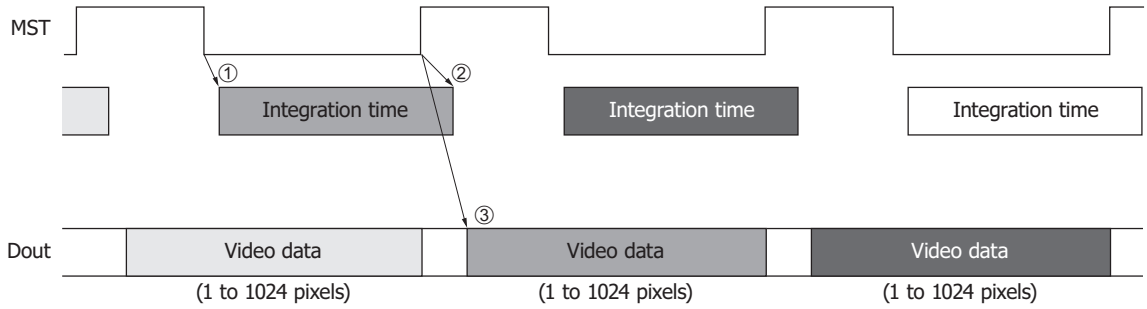
Parameter	Symbol	Min.	Typ.	Max.	Unit
Master start pulse period*13 *14	tpi(MST)	1162/f(MCLK)	-	-	s
Master start pulse high period	thp(MST)	167/f(MCLK)	-	-	s
Master start pulse low period*15	tlp(MST)	16/f(MCLK)	-	-	s
Master start pulse rise and fall times	tr(MST), tf(MST)	-	5	7	ns
Master clock pulse duty	-	45	50	55	%
Master clock pulse rise and fall times	tr(MCLK), tf(MCLK)	-	5	7	ns

*13: When 1024 pixels are read out
*14: The period is (138 + N)/f(MCLK) when N pixels are read out.
*15: The integration time corresponds to the low period of the master start pulse + 43 cycles of MCLK. The integration time can be changed by changing the ratio of the high and low periods of master start pulse. If the first Pclk after the master start pulse goes high is assumed to be the first edge, the video signal output is started at the 148th falling edge of Pclk. Since the start of the video output is simultaneous with the rising edge of Sync, acquire the video signal in reference to Sync.

■ Description of operation

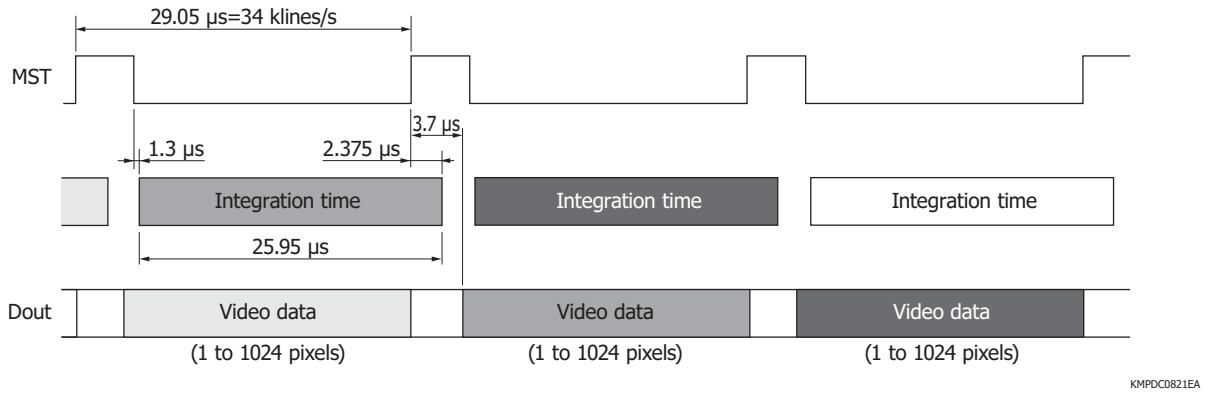
The integration time is determined by the low period of the master start pulse.



① The start of integration time is determined by the falling edge of the master start pulse.
② The end of integration time is determined by the rising edge of the master start pulse.
③ Video data is output after the rising edge of the master start pulse. Video data is output in order from the first pixel.
Note: Signal integration is possible even during video data output.

Operation example

Line rate=34 klines/s, master start pulse frequency=40 MHz, maximum integration time



· Master start pulse period=1162/f(MCLK)=29.05 µs (line rate is reciprocal of start pulse period)
· Master start pulse low period=Master start pulse period - Minimum period of master start pulse high period
=1162/f(MCLK) - 167/f(MCLK)=1162/40 MHz - 167/40 MHz=995/40 MHz=24.875 µs
· Integration time=Master start pulse low period + Master clock pulse 43 cycles=(995 + 43)/40 MHz=25.95 µs
Sync rises approximately 3.7 µs after the rising edge of the master start pulse. Then the video output signal is output in order from the first pixel.

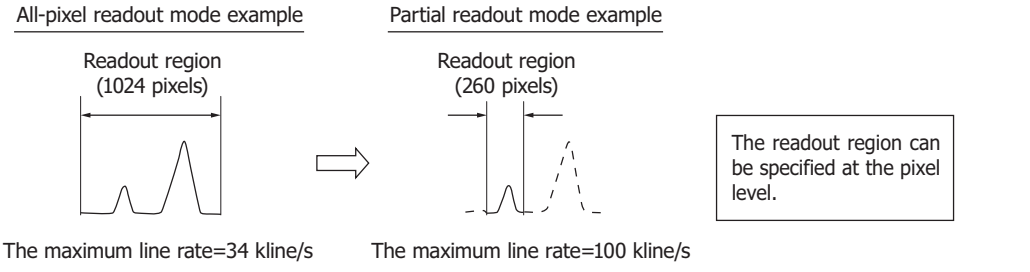
SPI (serial peripheral interface) address

Address (decimal)	Register	Initial value		Setting
		Binary	Decimal	
11	Win_S[10:8]	---- 0000	0	Readout start pixel (11-bit) (Initial setting: 0)
12	Win_S[7:0]	0000 0000		
15	Win_W[10:8]	---- 0100	1024	Number of readout pixels (11-bit) (Initial setting: 1024)
16	Win_W[7:0]	0000 0000		
18	SubsH[1:0]	---- --00	0	Number of skipped pixels (2-bit) (Initial setting: 0)
22	Offset[3:0]	---- 0111	7	Offset shift (4-bit) (Initial setting: 7)

Note: Be sure to set the addresses shown in the above table. Setting to the addresses not shown in the above table may cause malfunction.

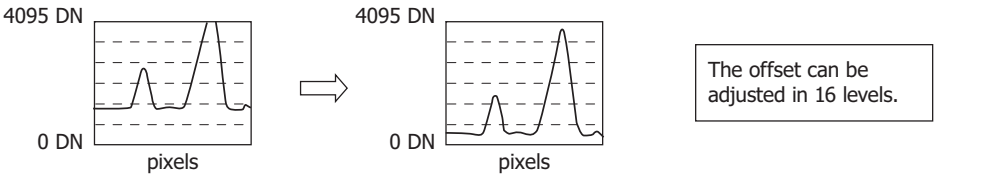
■ Setting the partial readout region

The partial readout region can be specified at the pixel level. The line rate can be increased by reducing the number of readout pixels.



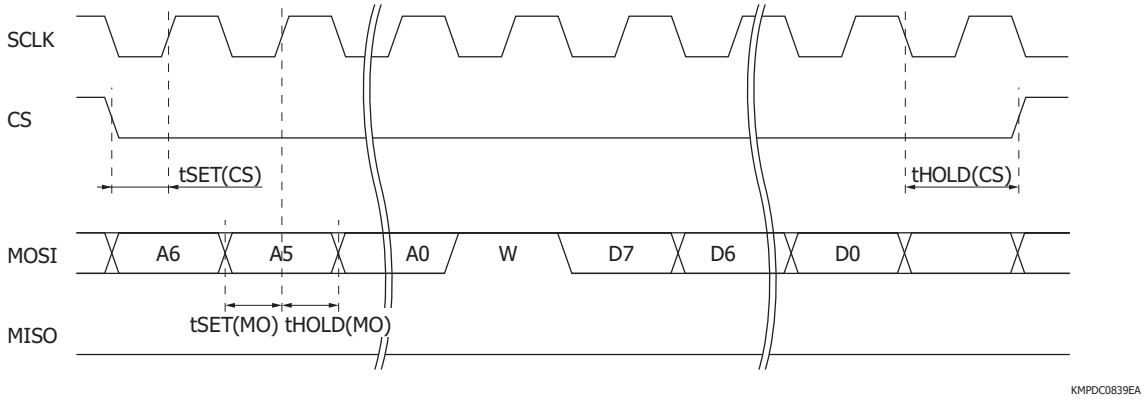
■ Setting the offset

The offset can be adjusted in 16 levels. The conversion range of the A/D converter can be used effectively by setting the appropriate offset.



Setting using the SPI

Set the SPI using SCLK, CS, and MOSI. Changing RSTB to low level resets all parameters to the initial settings.



KMPDC0839EA

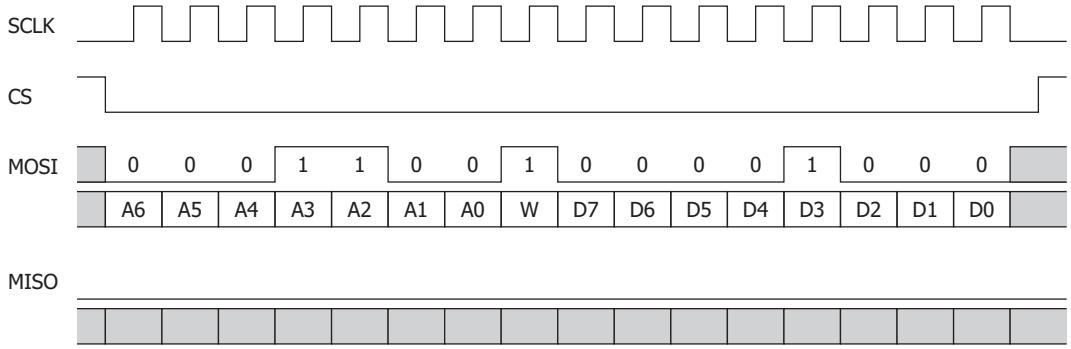
[Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock pulse frequency	f(SCLK)	-	7.5	10	MHz
SPI setup time (CS)	tSET(CS)	7	-	-	ns
SPI hold time (CS)	tHOLD(CS)	7	-	-	ns
SPI setup time (MOSI)	tSET(MO)	7	-	-	ns
SPI hold time (MOSI)	tHOLD(MO)	7	-	-	ns
Digital input signal rise time*16	tr(sigi)	-	5	7	ns
Digital input signal fall time*16	tf(sigi)	-	5	7	ns

*16: Time for the input voltage to rise or fall between 10% and 90%

■ Setting example

Set Win_S[7:0]=8



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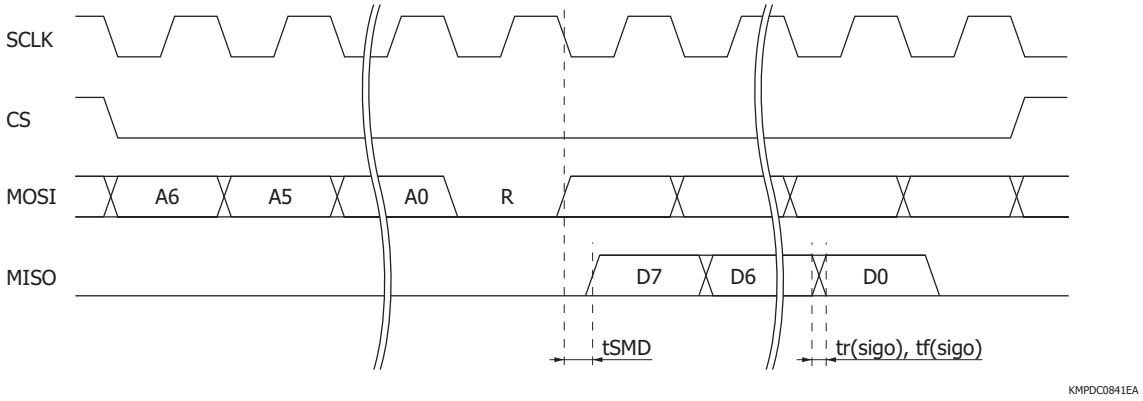
Confirm SPI settings

You can check the current SPI settings in the following manner.



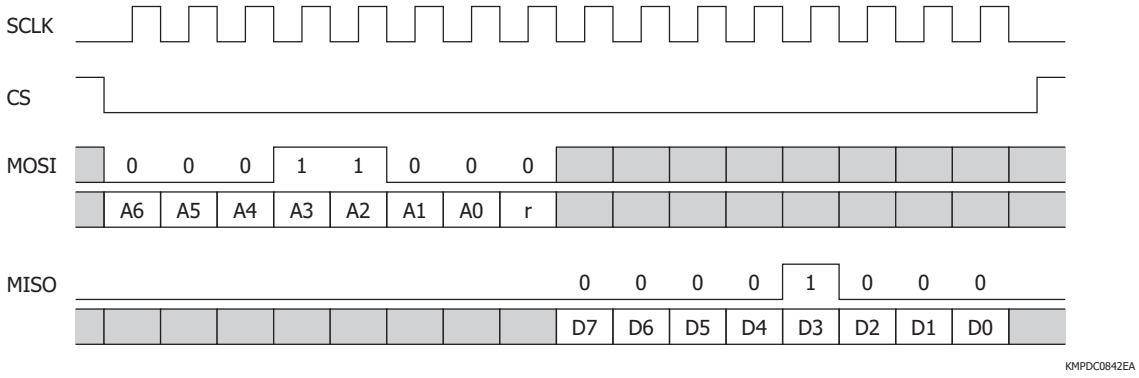
[Ta=25 °C, Vdd(A)=Vdd(D)=Vdd(C)=3.3 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output signal rise time*17	tr(sigo)	-	10	12	ns
Output signal fall time*17	tf(sigo)	-	10	12	ns
SCLK-MISO output delay time	tSMD	-	-	25	ns

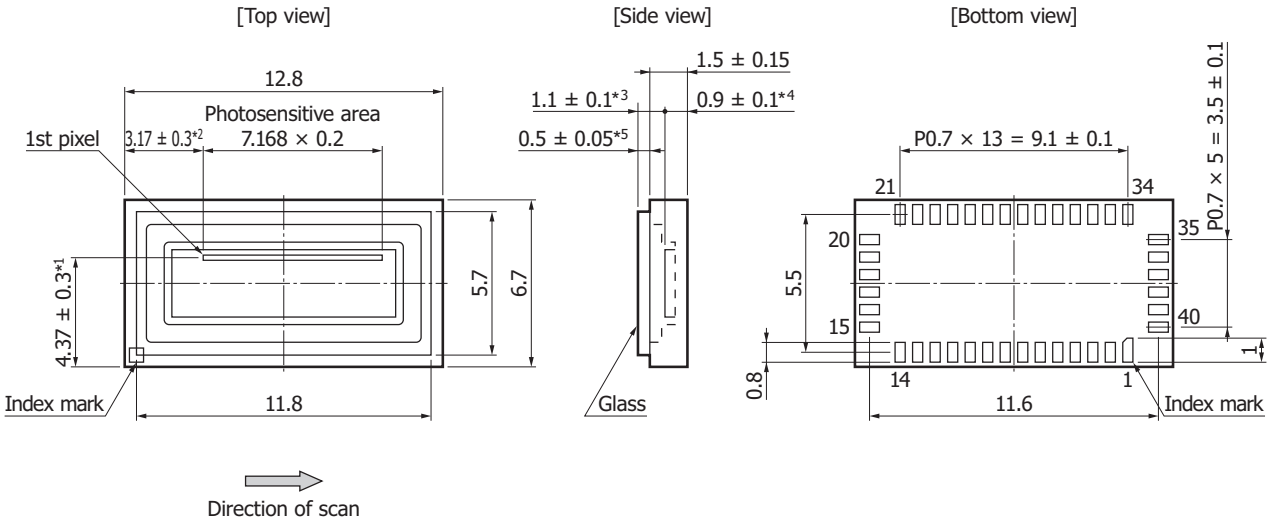
*17: Time for the output voltage to rise or fall between 10% and 90% when the load capacitance of the output terminal is 10 pF

■ Check example

Check Win_S[7:0]=8



Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.2
*1: Distance from package edge to photosensitive area center
*2: Distance from package edge to photosensitive area edge
*3: Distance from glass surface to photosensitive surface
*4: Distance from package bottom to photosensitive surface
*5: Glass thickness

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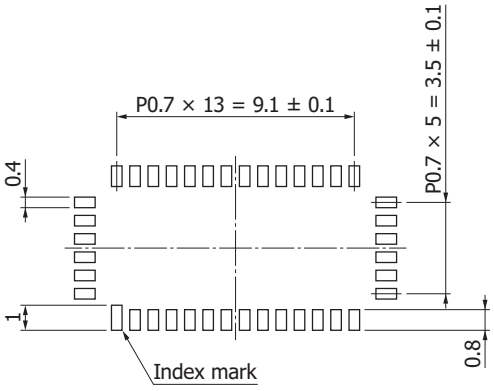
Recommended land pattern (unit: mm)



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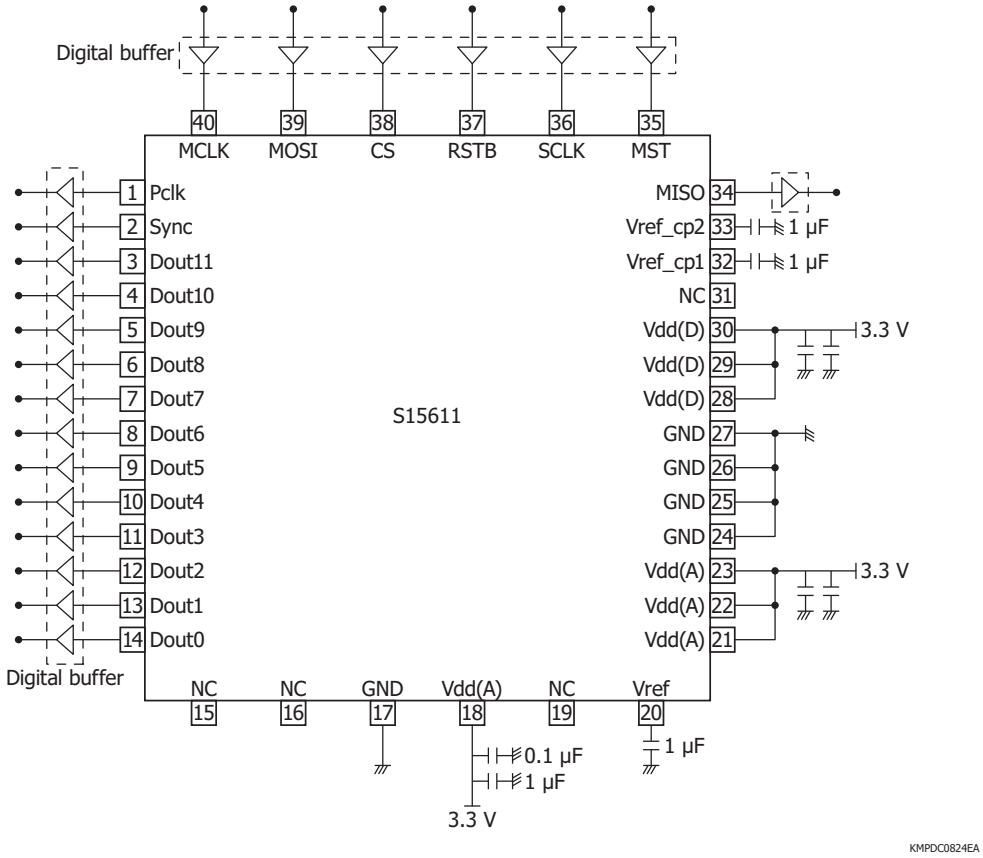
Application circuit example

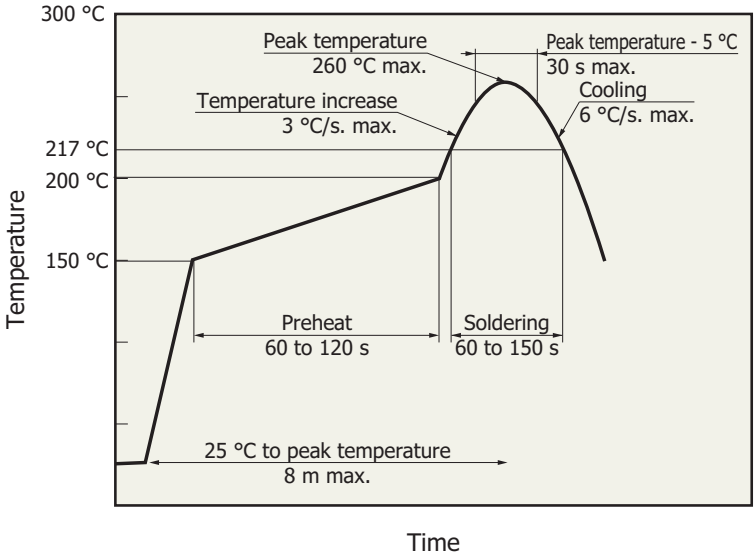


Pin connections

Pin no.	Symbol	Description	I/O
1	Pclk	Pixel output sync signal	O
2	Sync	Frame sync signal	O
3	Dout11	Video output signal (MSB)	O
4	Dout10	Video output signal	O
5	Dout9	Video output signal	O
6	Dout8	Video output signal	O
7	Dout7	Video output signal	O
8	Dout6	Video output signal	O
9	Dout5	Video output signal	O
10	Dout4	Video output signal	O
11	Dout3	Video output signal	O
12	Dout2	Video output signal	O
13	Dout1	Video output signal	O
14	Dout0	Video output signal (LSB)	O
15	NC*18	No connection	-
16	NC*18	No connection	-
17	GND	Ground	-
18	Vdd(A)	Analog supply voltage (3.3 V)	I
19	NC*18	No connection	-
20	Vref*19	Reference voltage	O
21	Vdd(A)	Analog supply voltage (3.3 V)	I
22	Vdd(A)	Analog supply voltage (3.3 V)	I
23	Vdd(A)	Analog supply voltage (3.3 V)	I
24	GND	Ground	-
25	GND	Ground	-
26	GND	Ground	-
27	GND	Ground	-
28	Vdd(D)	Digital supply voltage (3.3 V)	I
29	Vdd(D)	Digital supply voltage (3.3 V)	I
30	Vdd(D)	Digital supply voltage (3.3 V)	I
31	NC*18	No connection	-
32	Vref_cp1*19	Bias voltage for charge pump circuit	O
33	Vref_cp2*19	Bias voltage for negative voltage circuit	O
34	MISO	SPI output signal	O
35	MST	Master start signal	I
36	SCLK	SPI clock signal	I
37	RSTB	SPI reset signal	I
38	CS	SPI selection signal	I
39	MOSI	SPI input signal	I
40	MCLK	Master clock signal	I

*18: Leave NC pins open; do not connect to GND.
*19: Insert a 1 µF capacitor between the terminal and GND.

Recommended reflow soldering conditions (typical example)



KMPDB0405EA

· This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 72 hours.
· The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. When you set reflow soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.
· The bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

Precautions

(1) Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Input window

If dirt or dust adheres to the surface of the input window glass, the photoresponse uniformity will be lost. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use soft cloth, paper, a cotton swab, or the like moistened with alcohol to wipe off dust and stain. Then blow compressed air so that no stain remains.

(3) Operating and storage environments

Handle the device within the range of the absolute maximum ratings. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

(4) UV light irradiation

This product is not designed to resist characteristic deterioration under UV light irradiation. Do not apply UV light irradiation.

Related information

www.hamamatsu.com/sp/ssd/doc_ja.html

■ Precautions
· Disclaimer
· Image sensors
· Surface mount type products

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