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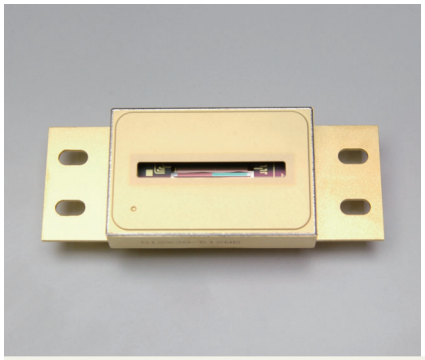
InGaAs linear image sensor



G12230-512WB

Employs two InGaAs chips (cutoff wavelength: 1.65 µm, 2.15 µm)
Near infrared image sensor (0.95 to 2.15 µm)

The G12230-512WB is an InGaAs linear image sensor designed for near infrared multichannel spectrophotometry. Two InGaAs chips with different cutoff wavelengths are arranged very accurately in series. The G12230-512WB provides high S/N over a wide spectral response range. The CMOS chip consists of charge amplifiers, a shift register, and a timing generator. Charge amplifiers are configured with CMOS transistor array and are connected to each pixel of the InGaAs photodiode array. Since the signal from each pixel is read in charge integration mode, high sensitivity and stable operation are attained in a wide spectral response range. The package is hermetically sealed providing excellent reliability.
The signal processing circuit on the CMOS chip enables the selection of an optimum conversion efficiency (CE) for your application from the available two types using external voltage.

Features

- **Employs two InGaAs chips**
- **Selectable from two conversion efficiency types**
- **Built-in saturation countermeasure circuit**
- **Built-in CDS circuit*1**
- **Built-in thermistor**
- **Easy operation (built-in timing generator*2)**
- **High resolution: 25 µm pitch**

Applications

- **Near infrared multichannel spectrophotometry**
- **Non-destructive inspection equipment**

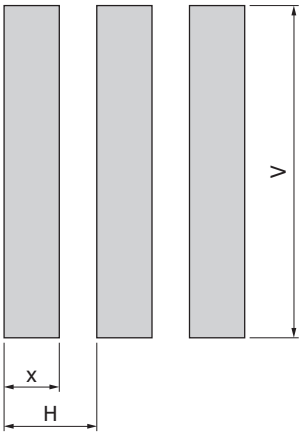
*1: A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. However, the CDS circuit, which takes the difference between the signal after the completion of the integration time and the signal immediately after resetting, greatly reduces the reset noise.

*2: Different signal timings must be properly set in order to operate a shift register. In conventional image sensor operation, external PLDs (programmable logic device) are used to input the required timing signals. However, the image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.

Structure

Parameter	Specification	Unit
Cooling	Two-stage TE-cooled	-
Image size	12.8 × 0.25	mm
Total number of pixels	512	-
Number of effective pixels	254 + 254	-
Pixel size (H × V)	25 × 250	µm
Pixel pitch	25	µm
Package	28-pin metal (refer to dimensional outline)	-
Window material	Sapphire (with anti-reflective coating)	-

Enlarged view of photosensitive area (unit: µm)



x	H	V
10	25	250

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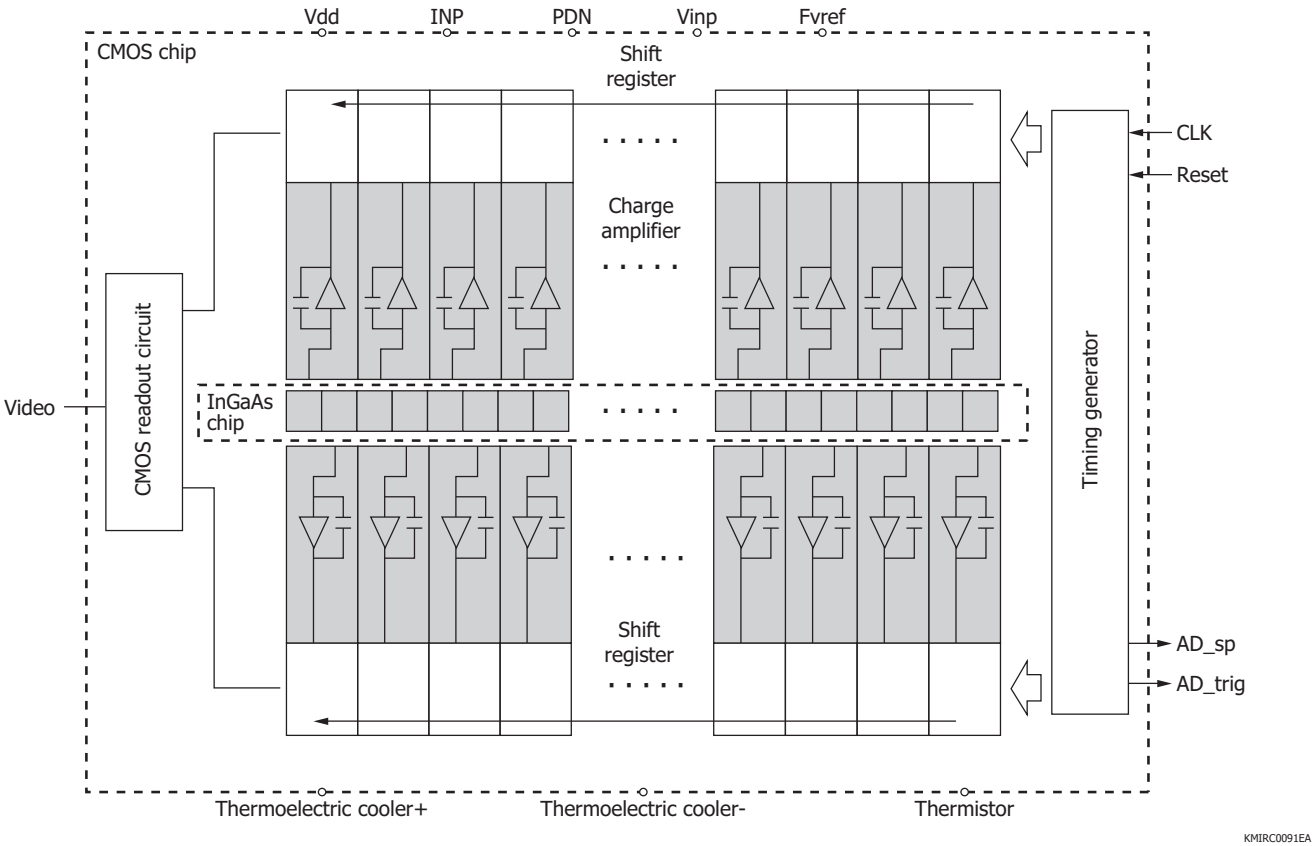
Block diagram



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Absolute maximum ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vdd, INP, Fvref Vinp, PDN	Ta=25 °C	-0.3	-	+6	V
Clock pulse voltage	Vclk	Ta=25 °C	-0.3	-	+6	V
Reset pulse voltage	V(res)	Ta=25 °C	-0.3	-	+6	V
Gain selection terminal voltage	Vcfsel	Ta=25 °C	-0.3	-	+6	V
Operating temperature*3	Topr	No dew condensation*4	-20	-	+70	°C
Storage temperature	Tstg	No dew condensation*4	-40	-	+85	°C
Soldering conditions	-		Up to 260 °C, up to 10 s			-

*3: Chip temperature and package temperature
*4: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.7	5.0	5.3	V
Differential reference voltage		Fvref	1.1	1.2	1.3	V
Video line reset voltage		Vinp	3.9	4.0	4.1	V
Input stage amplifier reference voltage		INP	3.9	4.0	4.1	V
Photodiode cathode voltage		PDN	3.9	4.0	4.1	V
Ground		GND	-	0	-	V
Clock pulse voltage	High	Vclk	4.7	5.0	5.3	V
	Low		0	0	0.4	
Reset pulse voltage	High	V(res)	4.7	5.0	5.3	V
	Low		0	0	0.3	

Electrical characteristics (Ta=25 °C)

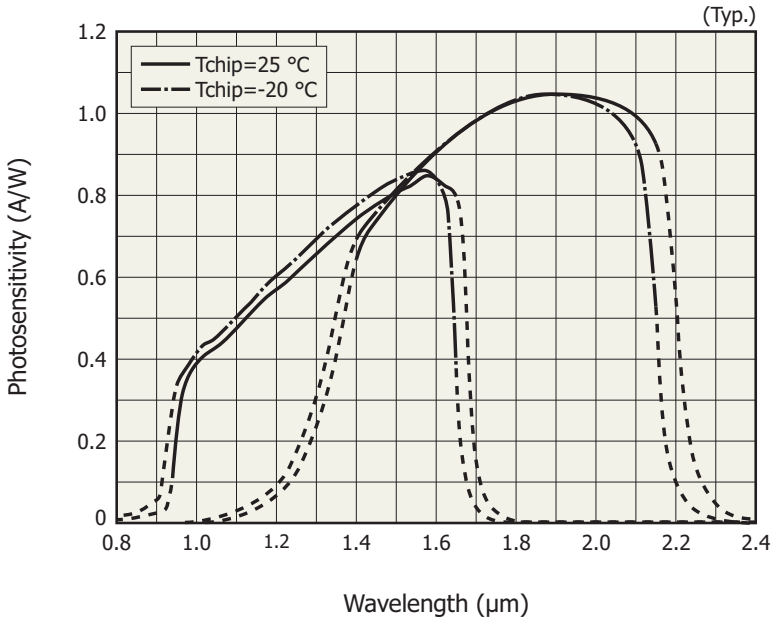
Parameter		Symbol	Min.	Typ.	Max.	Unit
Current consumption		I(Vdd)	-	80	100	mA
		Ifvref	-	-	1	
		Ivinp	-	-	1	
		Iinp	-	-	1	
		Ipdn	-	-	1	
Operation frequency		fop	0.1	1	5	MHz
Video data rate		DR	0.1	f	5	MHz
Video output voltage	High	V_H	-	3.9	-	V
	Low	V_L	-	1.2	-	
Output offset voltage		Vos	-	Fvref	-	V
Output impedance		Zo	-	5	-	kΩ
AD_trig, AD_sp pulse voltage	High	Vtrig, Vsp	-	Vdd	-	V
	Low		-	GND	-	

Electrical and optical characteristics (Ta=25 °C, Td=-20 °C, Vdd=5 V, INP=Vinp=PDN=4 V, Fvref=1.2 V, Vclk=5 V, fop=1 MHz)

Paramer	Symbol	Condition	Min.	Typ.	Max.	Unit
Spectral response range	λ	1 to 254 ch	-	0.95 to 1.65	-	μm
		259 to 512 ch	-	1.4 to 2.15	-	
Peak sensitivity wavelength	λp	1 to 254 ch	1.45	1.55	1.65	μm
		259 to 512 ch	1.8	1.95	2.05	
Photosensitivity	S	λ=λp, 1 to 254 ch	0.7	0.82	-	A/W
		λ=λp, 259 to 512 ch	0.85	1.0	-	
Conversion efficiency*5	CE	Cf=10 pF	-	16	-	nV/e⁻
		Cf=1 pF	-	160	-	
Photoresponse nonuniformity*6	PRNU		-	±5	±10	%
Full well capacity	Csat	CE=16 nV/e⁻	162.5	168.7	-	Me⁻
		CE=160 nV/e⁻	16.2	16.8	-	
Saturation output voltage	Vsat	CE=16 nV/e⁻	2.6	2.7	-	V
Dark output	VD	1 to 254 ch	-0.2	±0.02	0.2	V/s
		259 to 512 ch	-5	0.5	5	
Dark current	ID	1 to 254 ch	-2	±0.2	2	pA
		259 to 512 ch	-50	5	50	
Readout noise*7	Nread	CE=16 nV/e⁻	-	220	400	μV rms
		CE=160 nV/e⁻	-	300	500	
Dynamic range	Drange	CE=16 nV/e⁻	6500	12200	-	-
Defective pixels*8	-	CE=16 nV/e⁻	-	-	2	%

*5: For switching the conversion efficiency, see the pin connections.
*6: Measured at 50% saturation and 10 ms integration time after subtracting the dark output, excluding ch 1, 255 to 258, 512
*7: Integration time when CE=16 nV/e- is 10 ms. Integration time when CE=160 nV/e- is 1 ms.
*8: Pixels whose photoresponse nonuniformity, readout noise, or dark current is outside the specifications

Spectral response (typical example)



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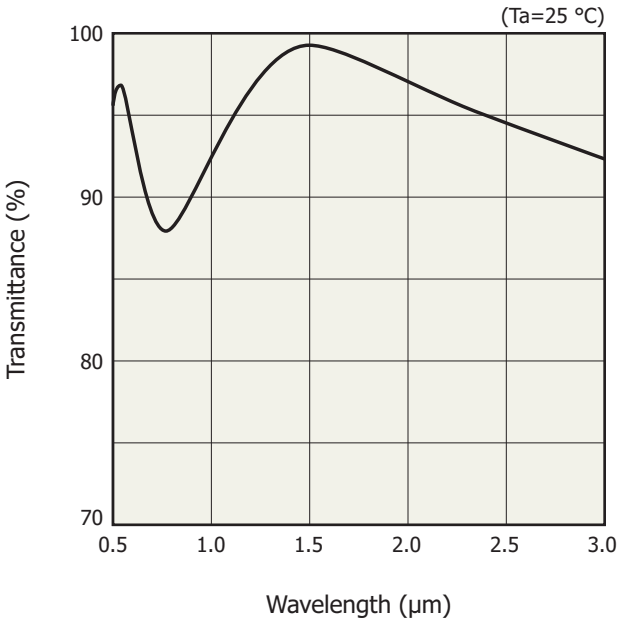
Spectral transmittance of window material (typical example)



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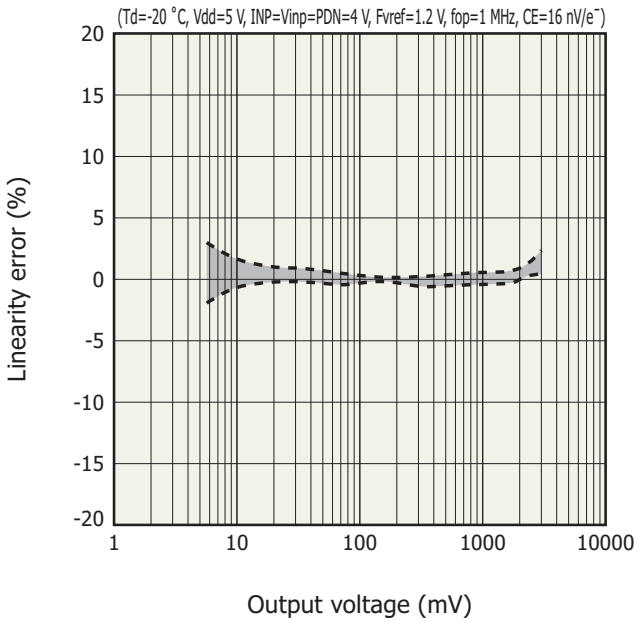
Linearity error



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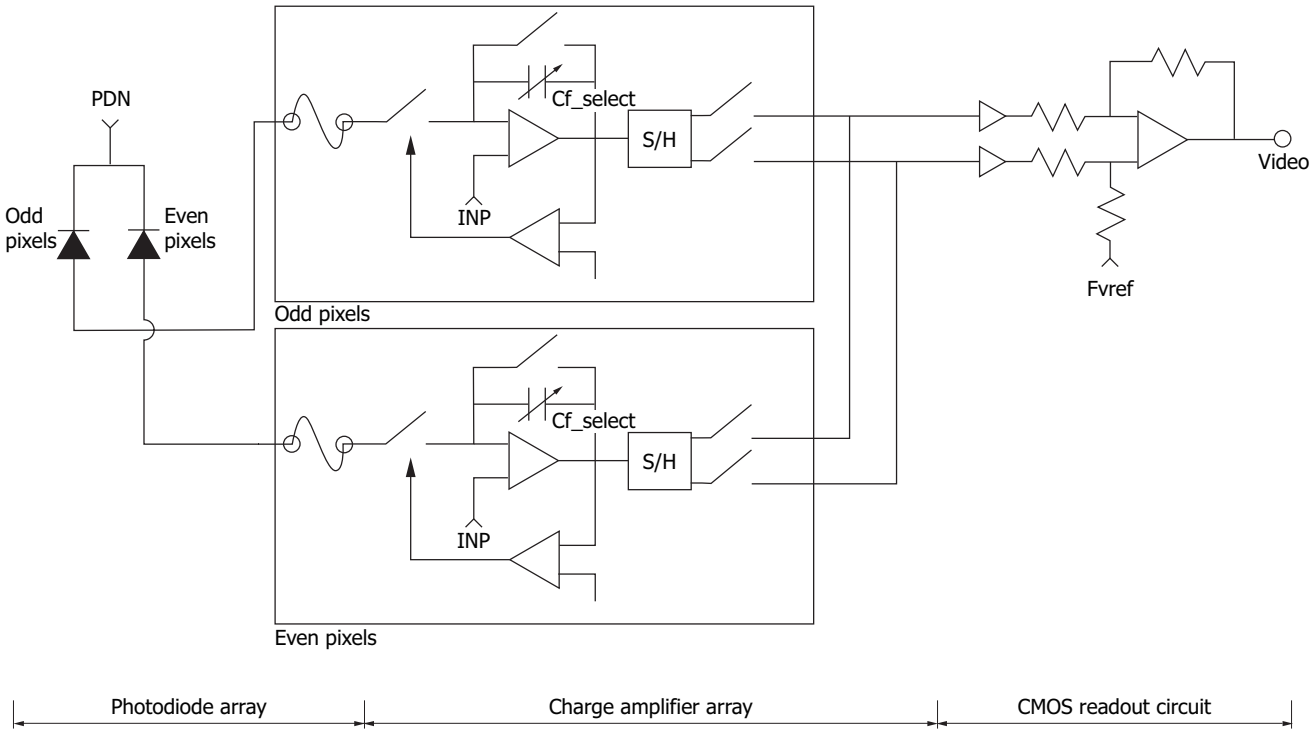
Equivalent circuit



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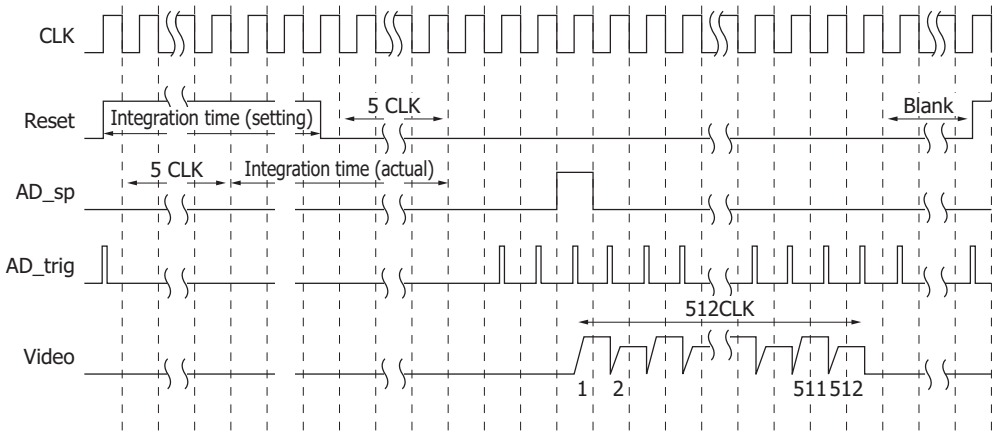
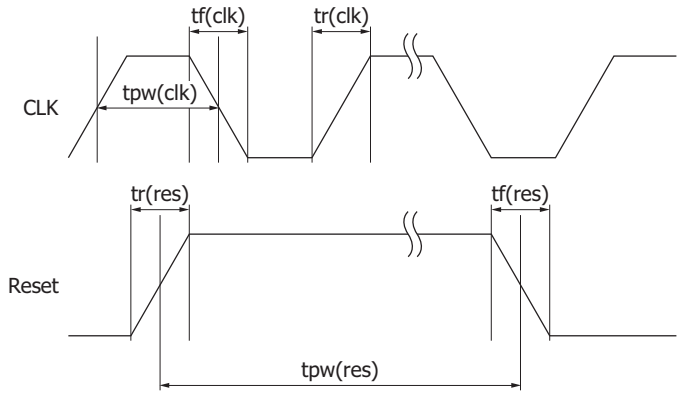
Timing chart





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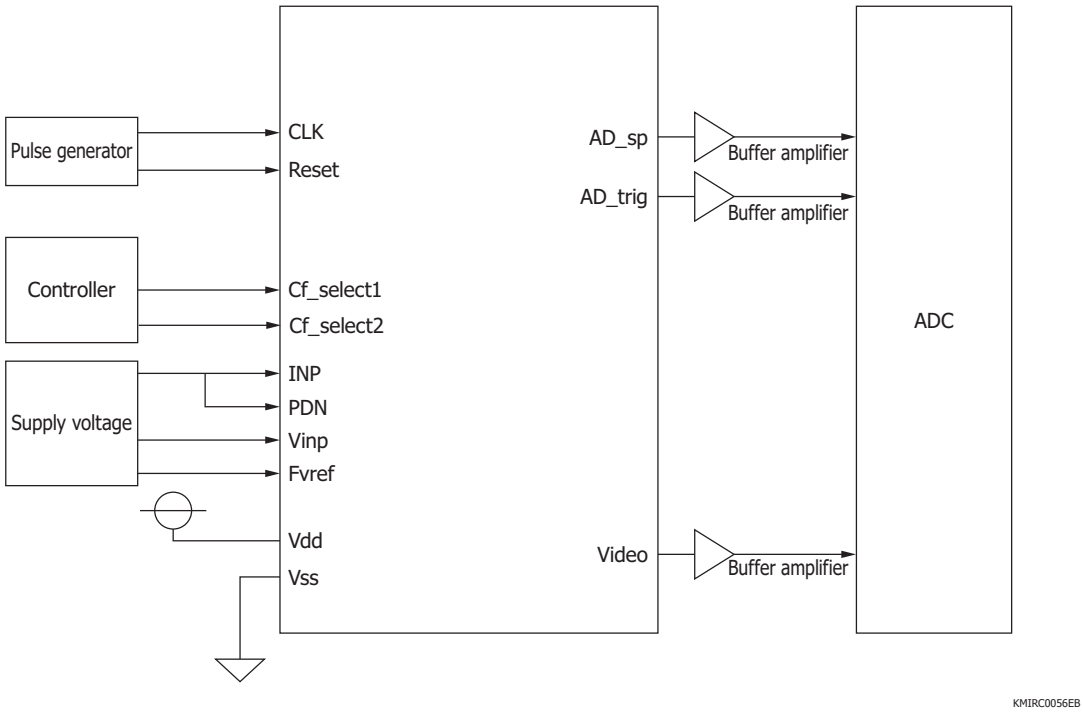
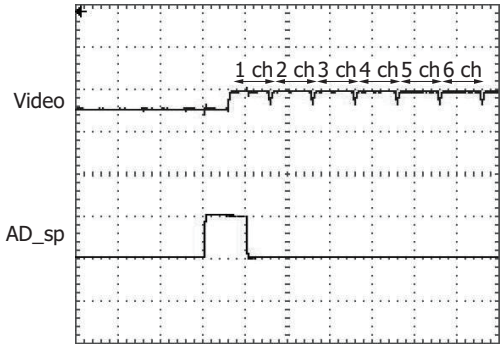
Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating frequency		fop	0.1	1	5	MHz
Clock pulse width		tpw(clk)	60	500	5000	ns
Clock pulse rise/fall times		tr(clk), tf(clk)	0	20	30	ns
Reset pulse width	High	tpw(res)	6	-	-	clocks
	Low		540	-	-	
Reset pulse rise/fall times		tr(res), tf(res)	0	20	30	ns

Connection example

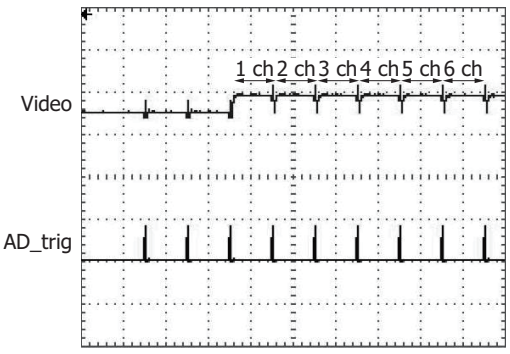


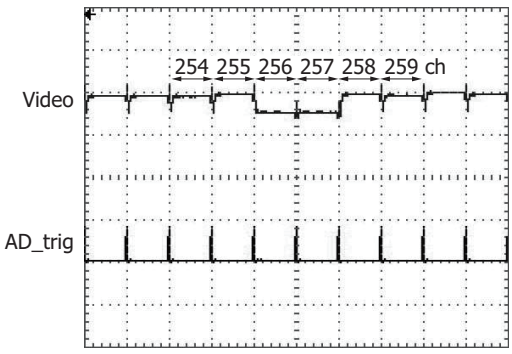
Output waveform of a pixel

■ Video & AD_sp



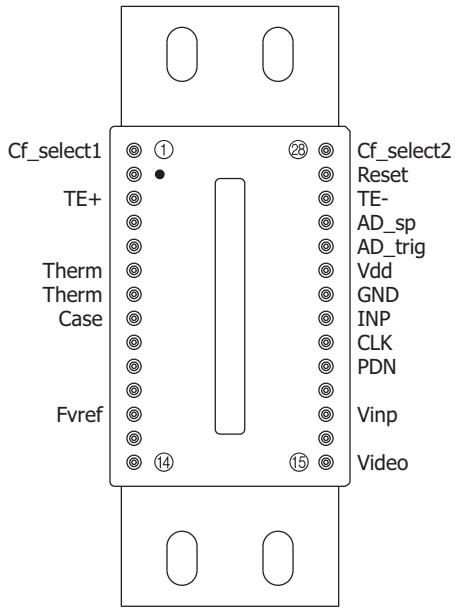
■ Video & AD_trig





No output from 256 and 257 ch

Pin connections (top view)



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Terminal name	Input/ output	Function and recommended connection	Remark
PDN	Input	InGaAs photodiode's cathode bias terminal. Set to the same potential as INP.	4.0 V
AD_sp	Output	Digital start signal for A/D conversion	0 to 5 V
Cf_select1, 2	Input*9	Signal for selecting the feedback capacitance (integration capacitance) on the CMOS chip	0 V or 5 V
Therm	Output	Thermistor for monitoring the temperature inside the package	-
AD_trig	Output	Sampling sync signal for A/D conversion	0 to 5 V
Reset	Input	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. Integration time is determined by the high level period of this pulse.	0 to 5 V
CLK	Input	Clock pulse for operating the CMOS shift register	0 to 5 V
INP	Input	Input stage amplifier reference voltage. This is the supply voltage for operating the signal processing circuit on the CMOS chip. Set to the same potential as PDN.	4.0 V
Vinp	Input	Video line reset voltage. This is the supply voltage for operating the signal processing circuit on the CMOS chip.	4.0 V
Fvref	Input	Differential amplifier reference voltage. This is the supply voltage for operating the signal processing circuit on the CMOS chip.	1.2 V
Video	Output	Differential amplifier output. This is an analog video signal.	1.2 to 3.9 V
Vdd	Input	Supply voltage (+5 V) for operating the signal processing circuit on the CMOS chip	5 V
GND	Input	Ground (0 V) for the signal processing circuit on the CMOS chip	0 V
Case	-	This terminal is connected to the package.	-
TE+, TE-	Input	Power supply terminal for the thermoelectric cooler for cooling the photodiode array	-

*9: The conversion efficiency is determined by the supply voltage to the Cf_select terminal as follows.

Conversion efficiency	Cf_select1	Cf_select2
16 nV/e^- (low gain)	High	High
160 nV/e^- (high gain)	High	Low

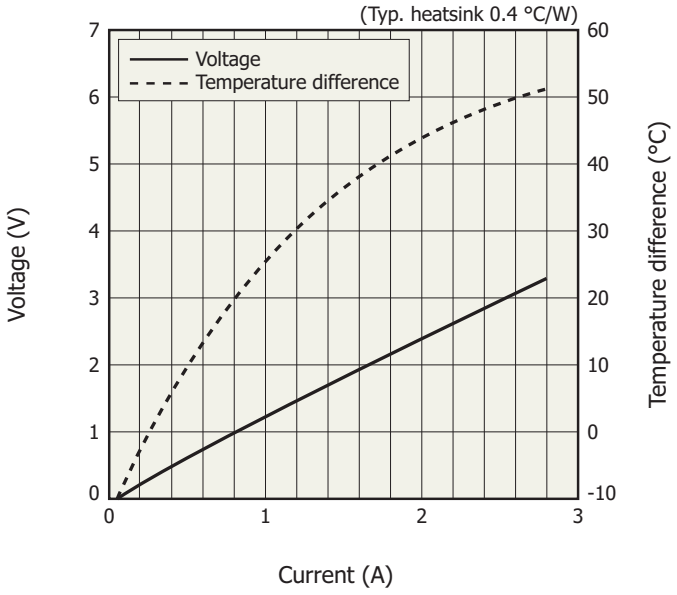
Low: 0 V (GND), High: 5 V (Vdd)

Specifications of TE-cooler (Ta=25 °C)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Allowable TE cooler current		Ic max	-	-	2.8	A
Allowable TE cooler voltage		Vc max	-	-	4.0	V
Temperature difference*10	Ic=2.6 A	ΔT	50	-	-	°C
Thermistor resistance		Rth	9	10	11	kΩ
Thermistor B constant	T1=25°C, T2=-20°C	B	-	3660	-	K
Thermistor power dissipation		Pth	-	-	400	mW

*10: Temperature difference between the photosensitive area and package heat dissipation area

TE-cooler temperature characteristics (Ta=25 °C, Vdd=5 V, INP=Vinp=PDN=4 V, Fvref=1.2 V, Vclk=5 V, fop=1 MHz)



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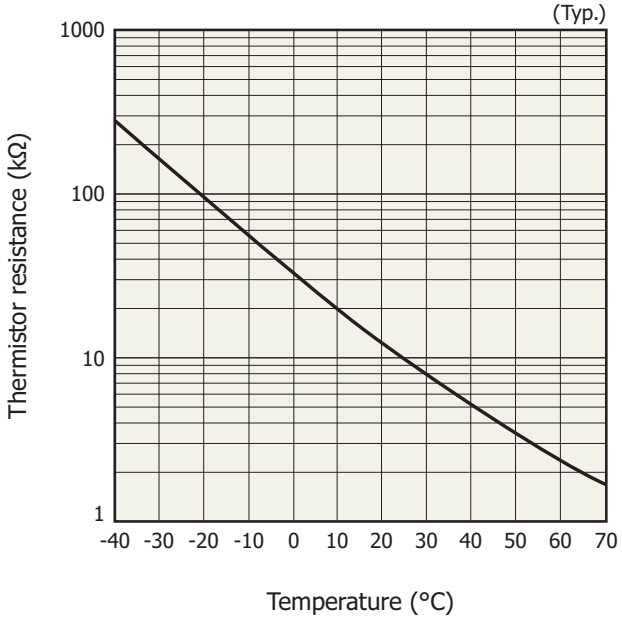
Thermistor temperature characteristics



Temperature (°C)	Thermistor resistance (kΩ)	Temperature (°C)	Thermistor resistance (kΩ)
-40	281	20	12.5
-35	208	25	10.0
-30	155	30	8.06
-25	117	35	6.53
-20	88.8	40	5.32
-15	68.4	45	4.36
-10	53.0	50	3.59
-5	41.2	55	2.97
0	32.1	60	2.47
5	25.1	65	2.07
10	19.8	70	1.74
15	15.7		

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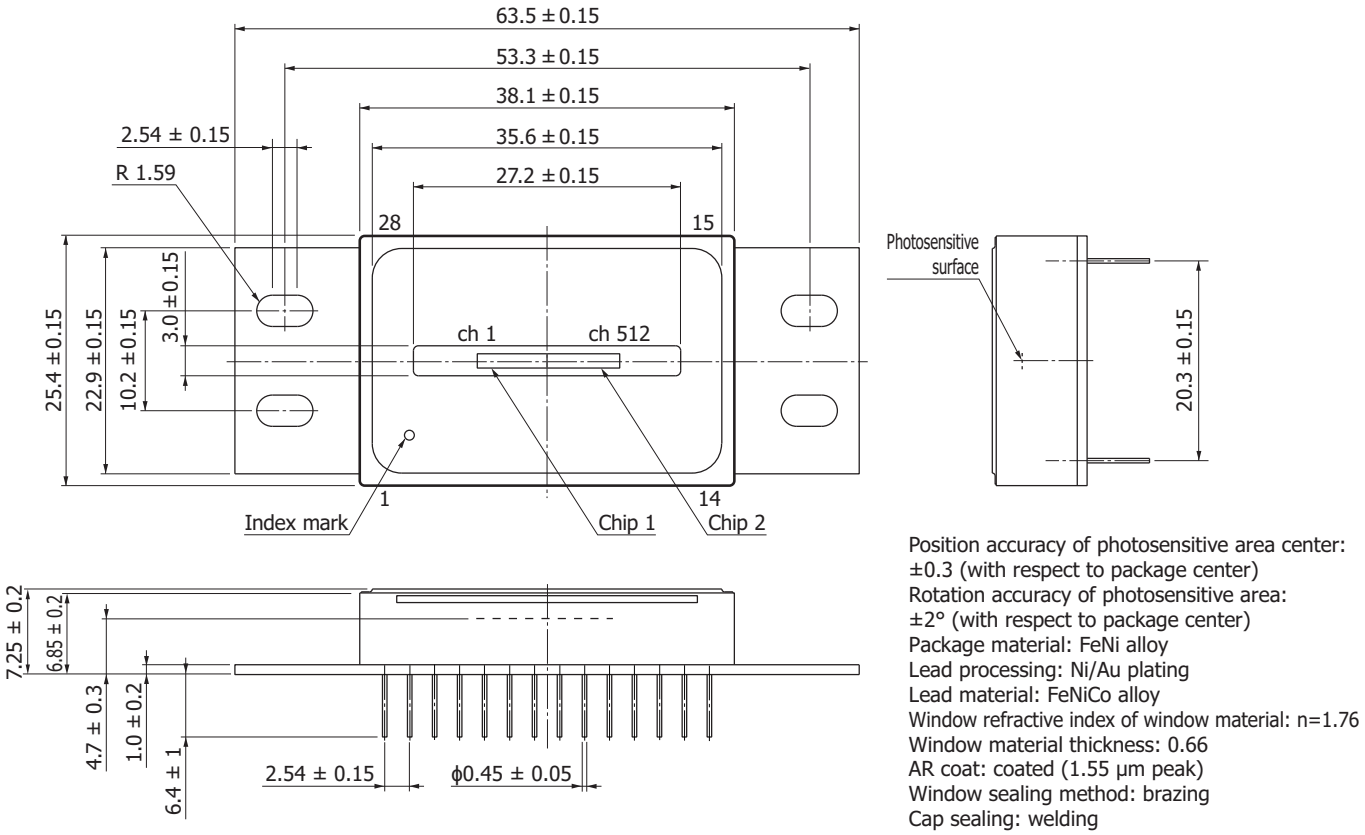
Dimensional outline (unit: mm)



Position accuracy of photosensitive area center: ±0.3 (with respect to package center)
Rotation accuracy of photosensitive area: ±2° (with respect to package center)
Package material: FeNi alloy
Lead processing: Ni/Au plating
Lead material: FeNiCo alloy
Window refractive index of window material: n=1.76
Window material thickness: 0.66
AR coat: coated (1.55 µm peak)
Window sealing method: brazing
Cap sealing: welding

	ch no.	Spectral response range
Chip 1	1 to 254	0.95 to 1.65 µm
Chip 2	259 to 512	1.4 to 2.15 µm

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Electrostatic countermeasures

This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Safety consideration
· Image sensors

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